A Stochastic Large-Signal Model for Printed High-Frequency Rectifiers Used for Efficient Generation of Higher Harmonics

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***Abstract*— This article investigates the stochastic Schottky barrier variations of printed distributed Schottky diodes consisting of a self-assembled arrangement of crystalline silicon microcones onto a metal layer. The microcone formation emerges from an inkjet printed Si nanoparticle film after laser sintering, yielding a Schottky diode when a corresponding top metallization is applied. The *I–V* characteristic and the voltage-dependent impedance of such diode is measured. By using the simulation software Advanced Design System (ADS), we develop a new scalable circuit model consisting of many different elementary diodes, which can explain the measured behavior. The elementary microcone diodes differ electrically in their barrier height, which is modeled as a stochastic process with a Gaussian distribution. A comparison between this model and a single diode model based on the thermionic field emission theory is conducted. We show that the distributed model outperforms the single-diode model in every regard and allows a prediction of the power levels of the harmonic frequency generation. Through more in-depth research, we find that a distributed barrier height leads to a smoother *I–V* curve, which in turn can lead to higher second and third harmonic power levels. By adjusting the barrier height distribution, the desired harmonics can be increased.**

***Index Terms*— Flexible printed circuits, radio frequency identification (RFID) tags, Schottky diodes, semiconductor device modeling, simulation.**

I. Introduction

CHIPLESS radio frequency identification (RFID) tags suffer from the problem of clutter, which means that their signal can be masked by reflections of the environment. However, when introducing a diode into the antenna structure of the tag, it can generate higher harmonic frequencies, allowing the backscattered signal of the tag to be distinguished from the environment [1]. However, such diodes have to be low-cost to manufacture and have a high switching speed to be integrated into RFID tags. In order to become inexpensive, printing processes are a suitable option due to their easy scalability for mass production. Various approaches and materials have been studied in the literature to realize a printable diode, but so far, none has been able to meet the requirements in terms of power, switching speed, or cost [2], [3]. Printable diodes based on Si particles offer the potential to overcome these shortcomings due to a high carrier mobility and Si being a highly available inexpensive material. An example is given in [4], where Si μ-particles have been employed to fabricate Schottky diodes in a printing process. The result is an ensemble of different elementary diodes, which represents a distributed type of Schottky diode. As indicated in [5], the barrier height can differ from diode to diode, even within the same process. These variations will likely be significantly larger in a distributed diode, meaning that the known Schottky diode models from the literature describing, e.g., the *I–V* characteristics or the frequency response are no longer applicable. Hence, there is a need for a comprehensive stochastic model for the new type of distributed Schottky diodes.

Following on from our previous work [6], this article briefly describes our approach to fabricate such diodes, which are here based on self-assembled crystalline silicon (c-Si) microcones, and explains our modeling efforts to characterize the electric behavior of these distributed diodes [7], [8]. In [7], we have set up a computational electromagnetics model based on the finite-element method (FEM) to estimate the parasitic capacitances, the parasitic resistances, and the potential cutoff frequency of such diodes. We developed a circuit model, where many different diodes are connected in parallel with the Schottky barrier height being formulated as a normally distributed random variable [8]. We then determined an effective distributed barrier height but without considering the capacitance. The distributed barrier height yielded an increase of the current for small input signal levels and thus resulted in higher levels of the generated harmonics, whereas the ratio of the fundamental level to the harmonic levels did not increase. The reason for this is that the fundamental level

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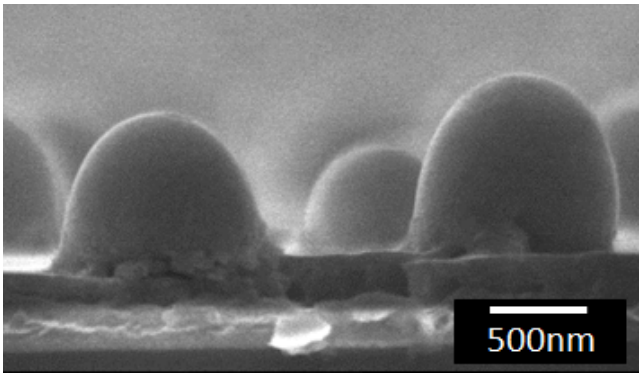

Fig. 1. Cross-cut scanning electron microscopy image of silicon microcones (from [8]).

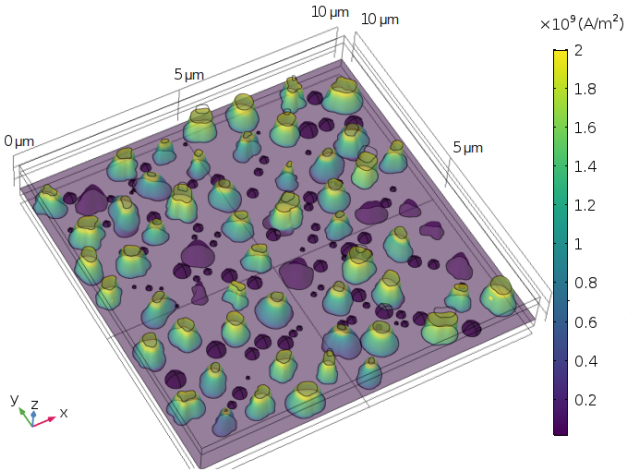

Fig. 2. Synthesized computational electromagnetic model of the distributed microcone arrangement for a representative area of 10×10 μm^2 displaying the norm of the current density at an operating frequency of 1 MHz (from [7]).

was considered too low due to the omission of the diode capacitance in the model. In this article, we introduce the diode capacitance and a parasitic geometric capacitance and extend the model to include the thermionic field emission theory. We fabricate three different distributed diode samples and test the presented model against the measurement data. This article is organized as follows. Section II gives a short description of the fabrication process of the printed diode. Section III then outlines the FEM model for the extraction of the parasitic values, and Section IV specifies the equations used for the stochastic circuit model. The validation of the proposed model against experimental data is presented in Section V. Using the stochastic model, we can predict the harmonic frequency generation of the printed diode, as shown in Section VI. Section VII deals with the effects of employing a diode with distributed barrier height and shows the potential of increasing the harmonic power levels. In the end, a conclusion is given in Section VIII.

II. Printed Diodes

Due to the possibility of simple upscaling, printing can lower the production costs per device. To further reduce the cost of printed RFID tags, they require being passive and chipless. However, these tags suffer from the problem of clutter where the environment masks the RFID signal and renders the tag useless. By integrating a printed diode, harmonic frequencies can be generated and backscattered, making the signal distinguishable from the environment. Thus, printed diodes enable cost-effective, high-performance RFID tags. For our approach to realize printable diodes [9], we utilize an ink containing silicon nanoparticles. In detail, p-doped silicon nanoparticles with a doping concentration of about 5×10^{17} cm^{-3} are first printed on a metal sheet and then laser sintered [6]. A detailed interplay of melting, cohesive forces, and thermal cooling take place and cause the nanoparticles to self-organize themselves into crystalline silicon (c-Si) conelike microstructures [10]. A scanning electron microscopy image of these microcones is shown in Fig. 1. The microcones provide a valuable structural precursor for printable high-speed Schottky diodes. By introducing a dielectric filling, together with a different top metallization, Schottky junctions will form, resulting in a distributed planar arrangement of many different elementary diodes connected in parallel (i.e., a diode array). The area covered by the top metallization determines the number of shunted elementary diodes and, thus, how large the current and capacitance of the total device will be. In this article, we choose a circular top metallization with a 1 mm diameter, resulting in a total area of 0.78 mm^2, encompassing approximately half a million elementary diodes.

III. Microcone Model

As a first modeling effort, SEM images of the silicon microcones are analyzed, with the goal to develop a stochastic representation for the shape of the microcones. With this representation, we create a synthesized geometric model of the microcone arrangement for the FEM solver COMSOL Multiphysics, which is described in more detail in [7]. In Fig. 2, the magnitude of the current density is shown when the model is excited by an ac voltage with a 1-V amplitude at 1 MHz. Due to the fabrication process, the microcones differ in height and it is, therefore, inevitable that not all of them can establish contact with the top electrode. Therefore, some cones do not carry current but still contribute to the capacitance (dark purple structures in Fig. 2). This is also the reason why such a model is needed, as the parasitic capacitance cannot be easily described by a plate capacitor but has to be extracted by an electrodynamic simulation. Due to limited computing resources, only a small piece of the total device is analyzed with an area of 10 μm $\times$ 10 μm. Such a device would contain around 140 different cone structures. This sample size is large enough to obtain a consistent parasitic capacitance of approximately 6.4 fF over several iterations of Monte Carlo-type simulations, each with randomly generated structures. However, as the fabricated diode consists of a total area of 0.78 mm^2, the parasitic capacitance of the sample device equates to 50 pF. This capacitance will be considered in the circuit model as a parallel capacitance C_{par} to the diode.

IV. Schottky Diode Model

With the increase of doping concentration in a Schottky junction, the probability of tunneling rises. The fabricated

diode exhibits a high enough doping concentration to be described by the thermionic field emission theory [11]. The thermionic field emission current is given by

$$I = I_s \exp\left(\frac{V - IR_s}{E_0}\right) \cdot \left[1 - \exp\left(-\frac{V - IR_s}{V_{\text{th}}}\right)\right] \quad (1)$$

with the saturation current

$$I_s = AA^*T^2 \exp\left(\frac{-\xi}{V_{\text{th}}}\right) \frac{\sqrt{\pi E_{00}(\phi_b - V - \xi)}}{V_{\text{th}} \cdot \cosh\left(\frac{E_{00}}{V_{\text{th}}}\right)} \exp\left(\frac{-\phi_b + \xi}{E_0}\right) \quad (2)$$

where V is the forward bias and R_s stands for the series resistance of the semiconductor bulk and the ohmic contact so that IR_s accounts for the voltage drop across the series resistance. V_{th} is the thermal voltage, which amounts to approximately 26 mV at a temperature of 300 K. In addition, A represents the effective diode area, A^* equals the effective Richardson constant of 32 ($\text{A/cm}^2\ \text{K}^2$) for p-type Si [11], and ϕ describes the barrier height. ξ is the difference of the Fermi level and the top of the valence band energy. E_{00} represents the tunneling energy, which is mainly dependent on the doping concentration N_A and the effective mass m^* of the majority carriers

$$E_{00} = 18.5 \cdot 10^{-15} \sqrt{\frac{N_A}{m^* \epsilon_r}}. \quad (3)$$

The abbreviation E_0 is used to set the tunneling energy E_{00} in relation to the thermal voltage.

$$E_0 = E_{00} \cdot \coth\left(\frac{E_{00}}{V_{\text{th}}}\right). \quad (4)$$

With said equations, the forward current can be described. However, there is another effect that can modify the current behavior, especially for the reverse bias regime. Due to image and dipole forces at the silicon–metal junction, the barrier height is lowered by $\Delta\phi$ [12]

$$\Delta\phi = \sqrt{\frac{e \cdot E_{\max}}{4 \cdot \pi \cdot \epsilon_0 \epsilon_r}} + \alpha \cdot E_{\max} \quad (5)$$

where e stands for the electron charge, ϵ_0 for the electric field constant, and ϵ_r is the relative permittivity of silicon, i.e., 11.9. The first term describes the barrier lowering due to image forces at the metal–semiconductor interface. The second term relates to the dipole force phenomenon described in [13], where α is an empirical factor. $E_{\max}$ denotes the maximum value of the electric field strength within the Schottky barrier. It can be estimated by applying the depletion approximation [14]

$$E_{\max} = \sqrt{\frac{2 \cdot e \cdot N_A \cdot |\phi_b - \xi - V - V_{th}|}{\epsilon_0 \epsilon_r}}. \quad (6)$$

To complete the diode model, the capacitance of the diode junction has to be included, which is approximated using a parallel plate capacitor model

$$C_d = \epsilon_0 \epsilon_r \frac{A}{W_d} \quad (7)$$

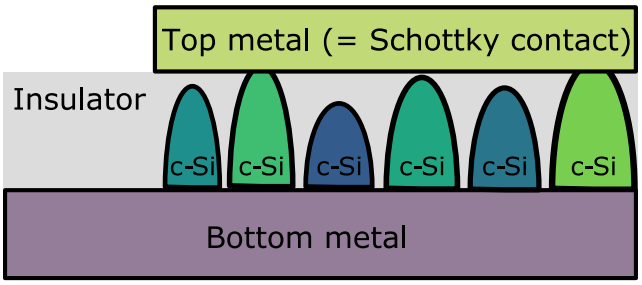

Fig. 3. Schematic cross-cut view of the distributed diode.

with the depletion width W_d.

$$W_d = \sqrt{\frac{2 \cdot \epsilon_0 \epsilon_r \cdot (\phi_b - \xi - V - V_{\text{th}})}{e \cdot N_A}}. \quad (8)$$

The depletion width is a function of the applied bias voltage V, yielding a voltage-dependent diode capacitance. With these equations, a large-signal model of the Schottky diode can be set up. As shown in [5], the barrier height ϕ_b of each diode can vary even for planar-processed diodes. The fabrication of distributed Schottky diodes encompassing microcones is a highly stochastic process, where the barrier height will undergo even larger variations. The current through each elementary diode is described by (1) and (2), with its corresponding values for $\phi_{b,n}$ and $R_{s,n}$. To represent the stochastic nature of the microcones, the barrier height is modeled as a random variable following a certain distribution. To point this out more clearly, a schematic cross-cut view of the distributed diode is shown in Fig. 3. It can be observed that each cone has a different geometric form [7]. As for this first modeling effort, we assume that in the fabrication process, the shaping of each cone is random and independent of other cones. Hence, each cone represents a unique elementary Schottky diode because each junction has a different shape and contact area, and in some cases, the junction is interrupted by an insulator interfacial layer. In the literature, it was shown that, depending on the thickness, such an interfacial layer can heavily modify the barrier height [15]. This results that each cone or each Schottky junction presents a different barrier height. However, in sum, the total device consisting of many diodes in parallel exhibits a barrier height distribution. As already mentioned, in our approach, it is assumed that each cone and thus each junction are independent of each other. When applying the central limit theorem, it follows that the normalized sum of the random junctions will lead to a normal distribution of the barrier height. Therefore, the barrier height for each diode is modeled as a random variable according to a Gaussian distribution described by the mean value $\bar{\phi}$ and the standard deviation σ. The density of barriers (DOB) function of this distribution is described by (9), which gives the probability to find the barrier height x in the given distribution

$$\text{DOB} = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(x - \bar{\phi})^2}{2\sigma^2}\right). \quad (9)$$

It seems plausible that a large number of different diodes are required to properly represent the Gaussian distribution.

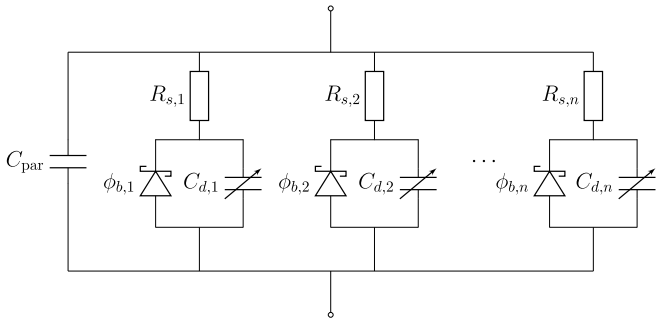

Fig. 4. Equivalent electrical circuit of the distributed Schottky diode encompassing the parallel connection of the corresponding elementary diodes (i.e., microcones).

Consequently, we use the scripting capabilities of the circuit simulation software Advanced Design System (ADS) to introduce a distributed Schottky diode encompassing 1000 different elementary diodes connected in parallel. The resulting electrical circuit of this overall device, including the parasitic capacitance C_{par} and the diode capacitance C_d and series resistance R_s of each elementary diode, is shown in Fig. 4.

V. Measurement and Simulation

To validate the presented distributed model, the characteristics of the fabricated diodes (see Section II) are measured. With the Keithley Model 4200-SCS Semiconductor Characterization System, the I–V characteristic in the range from -1 to $+1$ V is recorded. Furthermore, in a second measurement, the impedance of the distributed diode is measured at 0.1 MHz. Here, an ac signal of 10 mV is superimposed onto the bias, which is again swept from -1 to $+1$ V. The ADS random search optimization is used to fit the model to the measurement data and to find the proper parameters of the barrier height distribution. A dc simulation is utilized to match the I–V characteristic and, simultaneously, an ac simulation at 0.1 MHz is performed to confirm the impedance of the diode. This process is carried out for both, a model consisting of 1000 parallel diodes and a model of just one diode. The comparison between the two models and the measurement results is shown in Fig. 5, where the measurement is shown in green, the single diode model in red, and the distributed model consisting of 1000 diodes is shown in blue. As observed in Fig. 5(a), the current of the printed, distributed diode rises smoothly. An ordinary, single-diode I–V characteristic is expected to be sharper so that a clear threshold voltage can be defined. This is exactly what the single-diode model shows, though it cannot represent the real fabricated device. In the semilogarithmic plot of the I–V characteristic [see Fig. 5(b)], the discrepancy between the single-diode model and the measurement is even more evident. When the 1000-diode model that includes a barrier height distribution is applied, a very good agreement over a range from -1 to $+1$ V can be achieved. Fig. 5(c) shows a comparison between measured and simulated impedances. The real part is always positive and the imaginary part is always negative as the diode acts as a capacitance. Again, a significantly better agreement

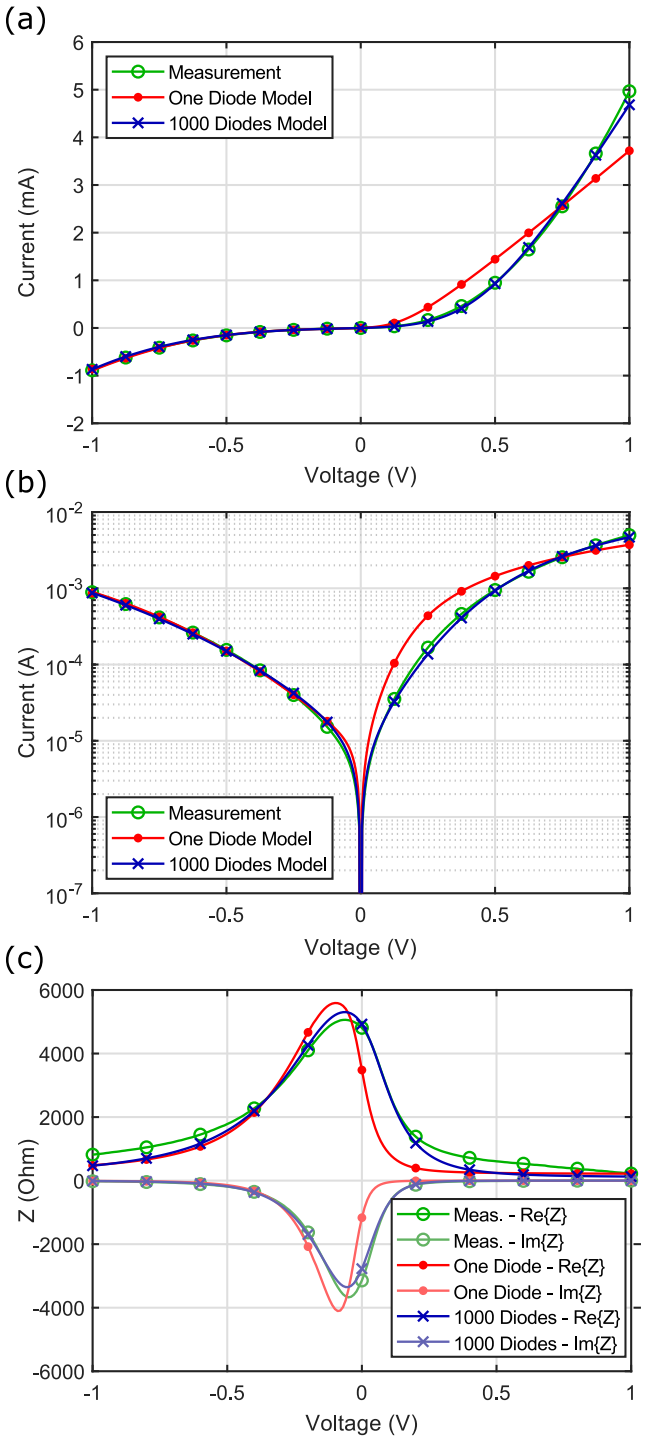

Fig. 5. Comparison between measurement and simulation model. (a) I–V characteristic in the linear plot. (b) I–V characteristic in the semilogarithmic plot. (c) Impedance at 0.1 MHz.

is achieved with the distributed model. For biases smaller than -0.4 V and larger than 0.2 V, the real part of the measured impedance and the modeled impedance starts to deviate. However, the precision of the model in terms of impedance is sufficient for our aim, namely to introduce this diode into printed chipless RFID tags. Therefore, the diode is typically operated in a zero-bias condition together with

TABLE I
MEASUREMENT OF THE HARMONIC POWER LEVELS AND COMPARISON OF THE SINGLE-DIODE AND DISTRIBUTED DIODE MODEL

		Measurement			Single Diode Model Error			Distributed Diode Model Error		
AC Voltage (V)	Frequency (MHz)	Fund. (dBm)	2nd Harm. (dBm)	3rd Harm. (dBm)	Fund. (dB)	2nd Harm. (dB)	3rd Harm. (dB)	Fund. (dB)	2nd Harm. (dB)	3rd Harm. (dB)
0.1	0.1	-47.3	-67.5	-76.3	-3.5	-12.4	-9.5	3.0	2.1	3.0
0.3	0.1	-33.6	-43.9	-49.2	-5.1	-7.8	-4.0	2.0	1.8	1.5
0.1	0.5	-37.9	-66.9	-76.3	2.9	-11.6	-9.1	4.8	2.2	3.1
0.3	0.5	-27.7	-44.1	-50.4	0.0	-8.0	-4.9	4.2	1.5	0.4
0.1	1	-33.3	-66.6	x	3.5	-10.8	x	4.0	1.5	x
0.3	1	-23.5	-44.3	-51.3	2.3	-7.9	-5.1	3.9	1.1	0.0
0.1	5	-23.3	-67.3	x	2.6	-3.7	x	1.6	-1.9	x
0.3	5	-13.8	-48.0	-59.3	2.9	-4.9	-3.3	1.7	-2.0	1.9
0.1	10	-20.4	-70.3	x	2.8	2.5	x	1.2	-0.2	x
0.3	10	-10.9	-52.3	-71.6	2.8	1.1	0.8	1.2	-1.2	3.5
0.1	15	-19.2	-73.6	x	2.8	8	x	1.3	2.1	x
0.3	15	-10.2	-56.0	x	2.3	5.3	x	0.7	0.6	x
0.1	20	-18.6	-78.5	x	2.6	12.7	x	1.3	2.9	x
0.3	20	-9.8	-60.1	x	1.9	10.4	x	0.6	1.8	x

a small-signal excitation. The model parameters found by the ADS optimization are worthy of mention. The effective diode area A is at 0.01 mm^2 very small compared to the total area of the device. This indicates that only a small portion of the diodes exhibit a good contact. The mean barrier height $\bar{\phi}$ is found to be 1.023 eV with a standard deviation of $\sigma = 0.163$ eV. This example already shows that a wide range of different barrier heights (i.e., a considerable standard deviation) are required for the model representation of the measurement data.

VI. HARMONIC FREQUENCY GENERATION

The distributed diode model and the single-diode model are used in the following, to predict the amplitude of higher harmonic frequency conversion. For this purpose, a transient simulation is set up in ADS. The excitation is carried out via sinusoidal voltage source at different frequencies and with an amplitude of 10 and 300 mV, respectively. At a 50-Ω load resistance, the power is recorded, and using a simple Fourier transform, its frequency components are calculated. For comparison purposes, this experiment is also conducted in the laboratory. Using the HMF2550 Arbitrary Function Generator from HAMEG Instruments as a voltage source, the same fabricated diode as before is connected in series to generate harmonics. With the Anritsu MS2668C Spectrum Analyzer, the power levels of the harmonics are recorded. The measurement and simulation results are summarized in Table I. The measured values of the power levels of the fundamental, second, and third harmonic are displayed as absolute values in dBm. The simulation results of the single-diode model and the distributed 1000-diode model are shown adjacently. They are expressed in decibel, as the difference to the measured value, in order to compare the error of the two different prediction models. The "x" entries are the cases where the third-harmonic power levels were beneath the noise floor, which is located at -80 dBm. The results clearly reveal the superior performance of the distributed model. The single-diode model predicts the fundamental frequency power level fairly well within a maximum error of -5.1 dB. The second- and third- harmonic power levels, though, are estimated too low with error levels above -12.4 and -9.5 dB. The distributed model, on the other hand, provides an accurate prediction of the harmonic power levels at both signal amplitudes and the given frequencies. The biggest error of 4.8 dB occurs in the fundamental component at 0.5 MHz and 0.1 V. The second harmonic is predicted even better, as the error lies below 2.9 dB. The prediction of the third harmonic works similarly well, and here, the error is always below 3.5 dB. All in all, this indicates that a distributed barrier height can describe the behavior of these printed diodes with high accuracy. The measurement shows a significant rise in the fundamental power level and a drop of the harmonic levels for frequencies above 5 MHz. This behavior is common for all diodes, as with increasing frequency the displacement current through the parasitic capacitance increases and thus short-circuits the rectification part (see Fig. 4). Therefore, there is always a cutoff frequency where the displacement current, which only exhibits a fundamental component, begins to dominate. However, the diode can generate small harmonic power levels at frequencies up to 10 MHz. At an input voltage of 0.1 V at 10 MHz, the power of the second harmonic has dropped by -3 dB (from -67.3 to -70.3 dBm), and hence, we define 10 MHz as the cutoff frequency for this distributed diode. The low value of the cutoff frequency can be explained by the small portion of elementary diodes that exhibit a good top contact and the large parasitic capacitance of 50 pF. In further work, we will decrease the total area of the device and try to ensure a reliable contact to all diodes. In this regard, we estimated an increase in the cutoff frequency toward the multigigahertz range. With the validity of the model assured, the influence of the distributed barrier height can now be further analyzed by altering the standard deviation σ.

VII. DISCUSSION ON THE DISTRIBUTED BARRIER HEIGHT

In this section, we discuss what advantages and disadvantages a distributed diode exhibits. At first, we analyze the dc characteristic and the harmonic generation at an operating frequency well below the cutoff frequency. Three different diode models with different standard deviations of the barrier height σ are compared. We choose the same diode parameters as the fabricated diode and only change $\sigma = 0 \mid 0.1 \mid 0.2$ eV,

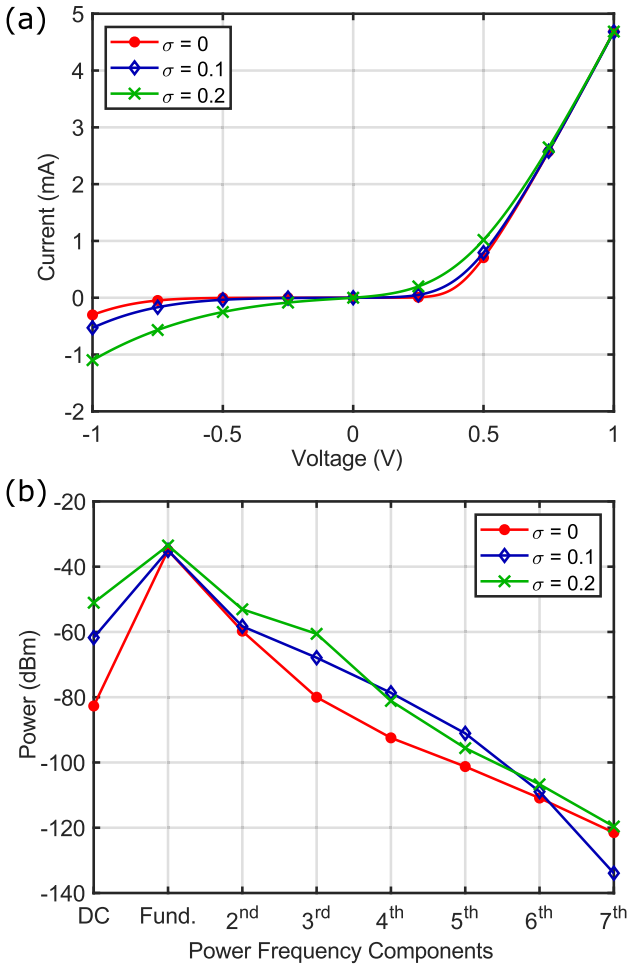

Fig. 6. Comparison of three distributed diodes with different standard deviations σ of the barrier height distribution. (a) I–V characteristic. (b) Frequency components obtained by a harmonic balance analysis. Input power of -10 dBm at 1 MHz.

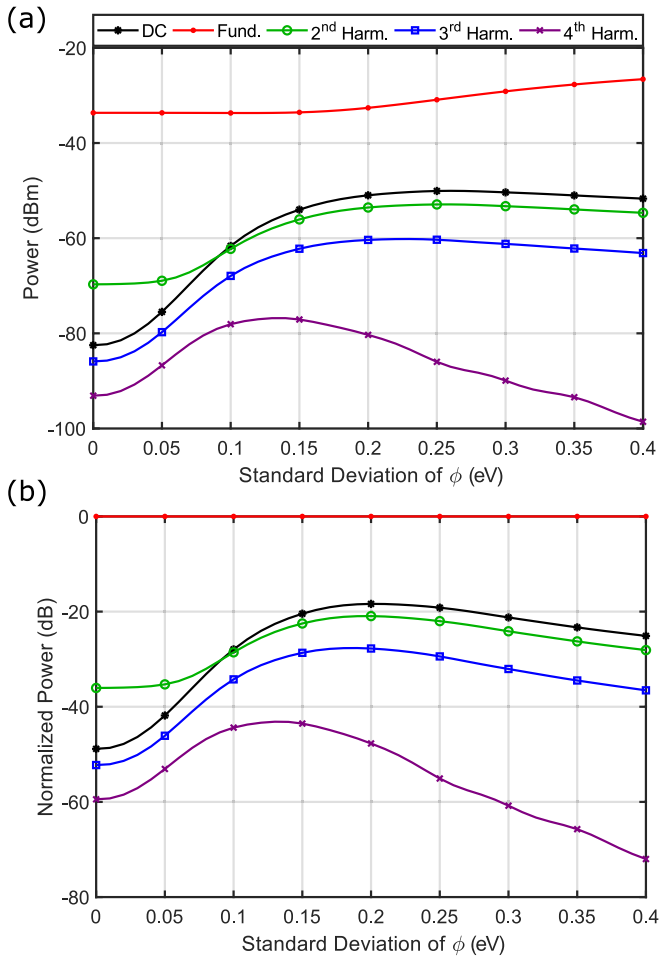

Fig. 7. Power levels of the harmonics and dc component of the rectified signal plotted against σ (standard deviation of the barrier height). (a) Absolute values. (b) Normalized to the absolute values of the fundamental component. Input power of -10 dBm at 1 MHz.

respectively, for the three models. A standard deviation of $\sigma = 0$ eV corresponds to the case of one single diode Because, in all the diodes, the barrier height is equal to the mean barrier height ($\phi_{b,n} = \bar{\phi}$). The result of the dc circuit simulation with a voltage sweep from -1 to 1 V is shown in Fig. 6(a). At high forward voltages, the I–V curves of the different diodes converge because the current is limited by the series resistance. However, it appears that this limiting effect occurs later with an increase in σ (as the curves rise more smoothly and display higher currents at lower voltages). At high values of σ, the I–V characteristic is more similar to a polynomial behavior than to an exponential behavior. In the case of a Taylor series expansion, the second- and third-order Taylor coefficients would be amplified, which would also increase the generation of the respective harmonics [16]. A detailed examination of this relationship can be found in the Appendix. This is a first surprising indication that distributed diodes with large intrinsic variations could have the potential to create larger second- and third-order harmonics for small input signal amplitudes, which could be beneficial, especially for applications in passive chipless RFID tags. To verify this assumption, harmonic balance simulations are conducted with a power source of -10 dBm at 1 MHz. A load resistance of 50 Ω is used to calculate the power frequency components and, thus, the harmonic generation capabilities of the distributed diodes. The dc current, the fundamental frequency, and the higher harmonics up to the seventh order are plotted in Fig. 6(b). As expected, most of the signal power is still carried by the fundamental frequency, but due to the rectification, there is a large proportion of dc and harmonic frequency components. In the presented case, the components generally rise with increasing standard deviation σ of the barrier height. However, the seventh harmonic is lowered when changing σ from 0 to 0.1 eV. In the case of $\sigma = 0.2$ eV, the power components rise again, but here the fourth and fifth components are lower than for $\sigma = 0.1$ eV. An explanation for this behavior could be that the higher order harmonics (from the fourth on) are now redistributed within the second and third harmonic. We assume that the amplitude of the frequency components could be tailored by changing σ. In order to investigate this assumption, more simulations are performed, where the frequency components are now inspected as a function of the barrier height's standard deviation σ. Fig. 7(a) shows the results of the harmonic balance simulation at 1 MHz.

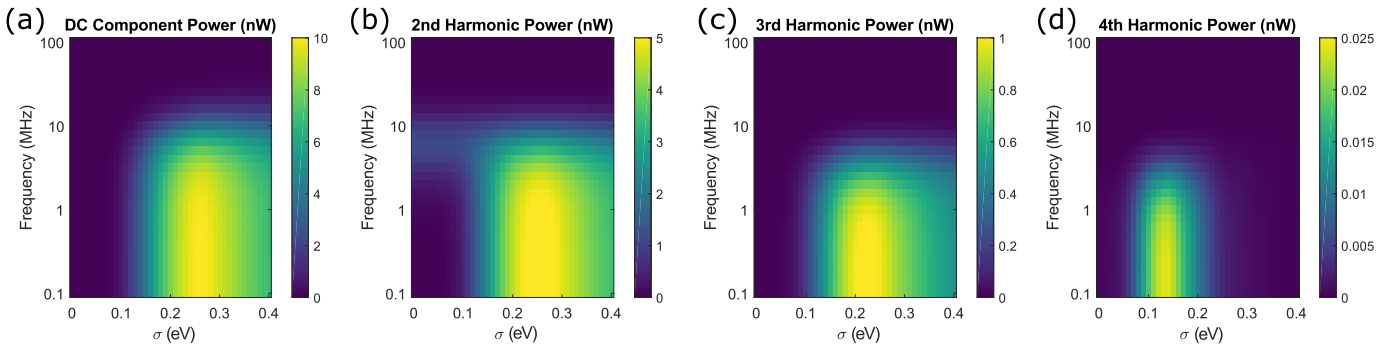

Fig. 8. Simulated power levels of the generated dc component and the harmonics for operating frequencies swept from 0.1 to 100 MHz and for changing standard deviation σ of the barrier height distribution. (a) DC component. (b) Second harmonic. (c) Third harmonic. (d) fourth harmonic.

As already mentioned, the harmonic components first rise with an increase in standard deviation and reach a maximum before decreasing again. This decrease is especially visible for the fourth harmonic and it supports the conjecture that the power of higher order harmonics will be redistributed to lower order harmonics. However, with an increase in σ, the probability of having more low barrier diodes increases, and as the barrier height of a diode declines, the nonlinear behavior of the device diminishes and only the series resistance will remain. Consequently, by increasing σ, more diodes will act as resistors while introducing linear current paths, enhancing the fundamental frequency component at the expense of the harmonics. This is a second effect that counteracts the first one, and it explains why the dc and the second- and third-harmonic components tend to be saturated. While this behavior can be an advantage for the outlined application scenario, the use of the distributed diode structure is not recommended for applications that require a sharp slope and a high ON/OFF ratio. This is because a large standard deviation of the barrier height leads to linear parallel paths and larger reverse currents, both of which reduce the ON/OFF ratio. When the power of the frequency components is plotted in relation to the fundamental component, as shown in Fig. 7(b), a similar behavior to Fig. 7(a) can be observed, albeit global maxima can be clearly identified. It shows that by choosing a specific standard deviation σ, the generation of harmonics can be optimized. To ensure that this optimization works for the whole operating frequency range of the distributed diode, further simulations are carried out. Now, a logarithmic frequency sweep from 0.1 to 100 MHz is added. The results are shown in Fig. 8, where a lighter color stands for a higher power at the corresponding harmonic frequency. The given distributed diode works well as a rectifier and harmonic frequency generator up to frequencies of approximately 10 MHz where the power of the frequency components remains constant. However, it can be seen that there is a strong dependence on the variation of the barrier height (i.e., σ). If a control of the barrier height distribution is given, the I–V characteristic can be adapted in such a way that the generation of a certain harmonic frequency is optimized. Both the dc component and second-harmonic component reach a maximum value for $\sigma = 0.26$ eV. Regarding the other components, the maxima are reached with the standard deviations of 0.23 eV (third harmonic) and 0.13 eV (fourth harmonic).

VIII. Conclusion

This article analyzes the effect of a distributed Schottky barrier on the higher harmonic generation. Here, the barrier height distribution is caused by the fabrication of a high-frequency rectifier using laser modified nanoparticles, which results in an ensemble of different microcone-shaped elementary diodes connected in parallel. This ensemble is modeled with an electrical equivalent circuit model, in which each elementary diode exhibits a different barrier height described by a normal Gaussian distribution. The I–V characteristic and the impedance of the fabricated distributed Schottky diode were measured, and the parameters of the model were adjusted to mimic the diode behavior. Thus, the model could then be used to predict the power level of the generated harmonics. Compared with a single-diode model, the proposed distributed model performed much better and was able to reproduce the measurement results with great accuracy. This leads us to the conclusion that a distributed barrier height is indeed present in this printed ensemble of elementary diodes based on nanoparticles. Therefore, it is useful to perform a theoretical evaluation that analyzes the effect of the distributed barrier height. With an increase in standard deviation, the I–V characteristic becomes smoother, and as a result, the overall turn-on voltage decreases. The smoother I–V behavior also changes the power level in the frequency components. For small amplitudes of the input signal, larger harmonic frequency components can be generated compared with a single diode.

In the literature, there is some discussion about what effects can influence the Schottky barrier height. Deviations from the Schottky–Mott rule are usually explained by the change of electron energy states, such as additional interface states or metal-induced gap states (MIGSs) [17]. Examples for the modification of Schottky barriers are given in [18] and [19], where a thin organic insulator film was inserted between the metal and the semiconductor. This could also be used in distributed diodes, where the thickness of the insulator layer could be varied depending on the location to tailor the barrier height distribution to application-specific needs. This plays an important role for the design of low-power RF circuits, such as, e.g., chipless RFID tags. There, the diode can be used to generate higher harmonics, which helps to circumvent the problem of clutter. By tailoring the barrier height distribution, the power levels of the generated harmonics could be enhanced and the range of the chipless RFID tag could be extended.

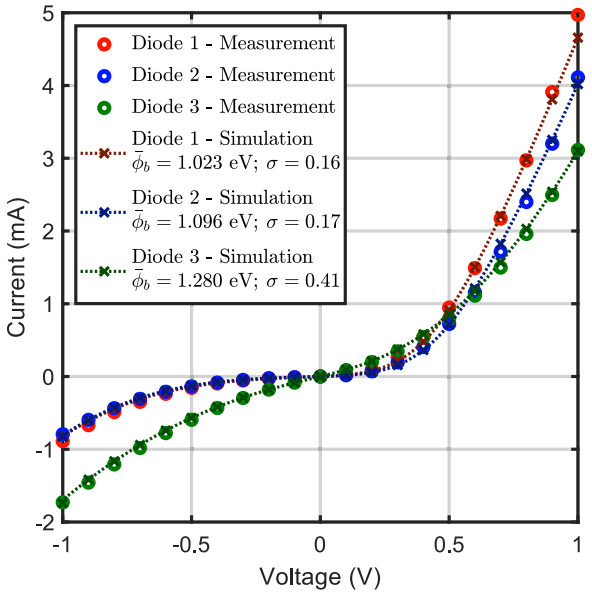

Fig. 9. Three different distributed diodes, fabricated with the same process parameters and respective simulated fit with the presented model.

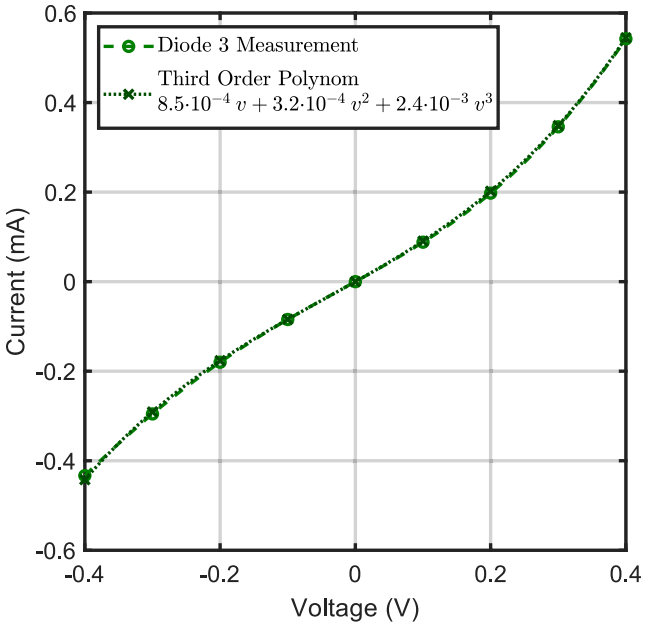

Fig. 10. I–V characteristic of third distributed diode sample and third-order polynomial fit.

Appendix
Relation Between I–V Characteristic and Harmonics

To verify the idea of a distributed barrier height spread across many different elementary diodes, we fabricated two additional samples of distributed diodes and discuss the different shapes of I–V curves in relation to the generation of harmonics. The measured I–V characteristics as well as the ADS dc simulation fit are shown in Fig. 9. The three different samples show a similar current level at 1 V, ranging from 3 to 5 mA. However, the shapes of the curves differ although they can be explained by different distributions of the barrier height. As can be seen, the proposed model offers a very good agreement to the measured data for all three samples. A lower current at high voltages, e.g., 1 V, is attributable to a higher mean barrier height $\bar{\phi}_b$, whereas a higher current at low voltages is due to a higher standard deviation σ in the barrier height. This can be clearly seen by examining diode sample 3, which shows a smooth current rise. Up to 0.4 V, the current of sample 3 exceeds the currents of the other samples but then falls short due to the higher mean barrier height. The reverse current is also higher for all voltage levels.

To discuss what the different distributions imply for the generation of harmonics, we consider an excitation ac signal given by

$$V(t) = V_{\mathrm{ss}} + \Delta V_{\mathrm{ss}} \cos(\omega t + \theta) \tag{10}$$

where V_{ss} is the dc-bias and ΔV_{ss} is the amplitude of the ac signal. Due to the nonlinear characteristic of the diode, the signal is distorted and contains harmonics of the excitation frequency. The ac current signal can then be expressed by a Fourier series

$$\begin{aligned} I(t) &= \sum_{n=0}^{\infty} I_n \cos(n\omega t + n\theta) \\ &= I_0 + I_1 \cos(\omega t + \theta) + I_2 \cos(2\omega t + 2\theta) \\ &\quad + I_3 \cos(3\omega t + 3\theta) + I_4 \cos(4\omega t + 4\theta) \ldots . \end{aligned} \tag{11}$$

The signal level of each frequency component is given by the coefficients of the Fourier series I_n. A direct connection of the Fourier coefficients and Taylor coefficients can be derived, allowing the signal levels of the harmonics to be determined from the I–V characteristic. In [16], a detailed derivation is given, and the even and odd harmonics can be calculated by the following equations:

$$I_{2n} = \sum_{m=n}^{\infty} \frac{1}{2^{2m-1}(m-n)!(m+n)!} \frac{d^{2m} I}{dV^{2m}}\bigg|_{V_{\mathrm{ss}}} (\Delta V_{\mathrm{ss}})^{2m} \tag{12}$$

$$I_{2n+1} = \sum_{m=n}^{\infty} \frac{1}{2^{2m}(m-n)!(m+n+1)!} \frac{d^{2m+1} I}{dV^{2m+1}}\bigg|_{V_{\mathrm{ss}}} (\Delta V_{\mathrm{ss}})^{2m+1}. \tag{13}$$

When approximating the I–V characteristic by a Taylor series around 0 V bias (e.g., up to the fifth order) with (14), the current of the second and third harmonic are then given by (15) and (16)

$$\begin{aligned} I(V(t)) &= c_0 + c_1\, V(t) + c_2\, V(t)^2 + c_3\, V(t)^3 \\ &\quad + c_4\, V(t)^4 + c_5\, V(t)^5 \end{aligned} \tag{14}$$

$$I_2 = \frac{1}{2} c_2 \Delta V_{\mathrm{ss}}^2 + \frac{1}{2} c_4 \Delta V_{\mathrm{ss}}^4 \tag{15}$$

$$I_3 = \frac{1}{4} c_3 \Delta V_{\mathrm{ss}}^3 + \frac{5}{16} c_5 \Delta V_{\mathrm{ss}}^5. \tag{16}$$

We consider only small input levels $\Delta V_{\mathrm{ss}} \ll 1$ V, which means that the power of ΔV_{ss} will be very small. Thus, the second harmonic depends mainly on the second Taylor coefficient, whereas the third harmonic depends mainly on the third Taylor coefficient. This leads to the conclusion that to maximize, e.g., the third-order harmonics, the shape of the I–V characteristic must resemble a rather polynomial shape, with a strong x^3 or a voltage to the power of 3 dependence. However, a single diode responds with an exponential behavior as described by

the thermionic field emission theory (see Sections I–V). The Taylor approximation of an exponential curve around $x = 0$ (i.e. Maclaurin Series) is given by

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} \dots . \tag{17}$$

Based on this infinite sum, it can be seen that a lot of high-order terms is needed to approximate the exponential curve and therefore to approximate the diode behavior. However, as the standard deviation of the barrier height increases, the I–V characteristic becomes smoother (see Fig. 6) and resembles a polynomial function with only low-order terms. To point this out, the characteristic of sample 3 for small input levels <0.4 V is shown in Fig. 10. The barrier distribution of this sample exhibits a standard deviation of $\sigma = 0.41$ eV, and it can be perfectly described by a third-order polynom. This is a good example showing how the contribution of high-order Taylor coefficients (from the fourth order on) lowers with rising standard deviation and how certain harmonics could be maximized by tailoring the barrier height distribution.

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