Performance optimization and process development of resonant-tunneling diodes for oscillator applications

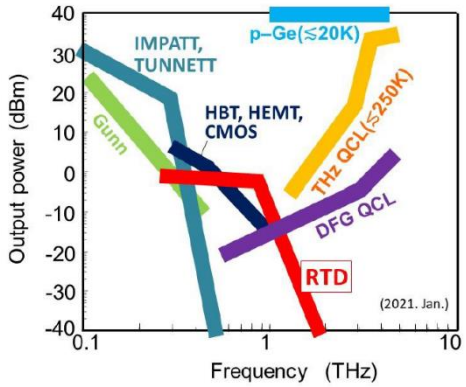

Fig. 1: *Comparison of available THz emitters [1]*

As the terahertz (THz) gap begins to close, enabling new applications in the areas of nondestructive evaluation and communication, sufficient output power especially around 1 to 2 THz remains challenging as can be seen in **Fig. 1**, which shows all available THz-sources. The resonant-tunneling diode (RTD) is a promising THz-oscillator as it is a simple and compact device which can easily be integrated into any circuit. It can operate at room temperature and is the fastest switching electrical semiconductor device.

The goal of this thesis is to increase the output power and general performance of a double barrier RTD structure by optimizing the layer stack. As a starting ground a design based on ref [2] is used, as it achieved 400 µW at 550 GHz.

Fig. 2 shows the main active part of the RTD which is a double potential barrier structure that forms a quantum well. Resonant tunneling occurs when the energy of an incident particle coincides with the quantized energy states of the quantum well. Applying a bias voltage therefore leads to an increase in current flow until it peaks when the energy level is aligned with the conduction band edge of the emitter. Further increasing the bias voltage results in a reduced current flow as resonant tunneling can no longer occur and less electrons are transmitted through the barrier structure. While the current is dropping the device is exhibiting a negative differential resistance (NDR) until it reaches a point where the current increases again due to

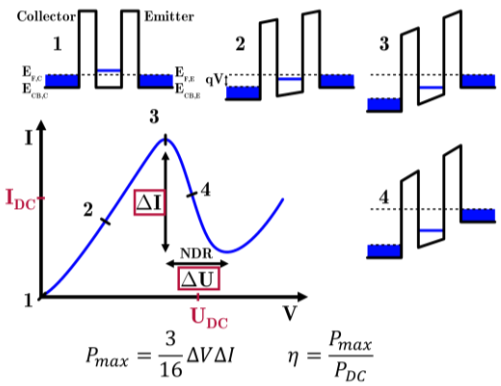

Fig. 2: *RTD band diagram and IV curve*

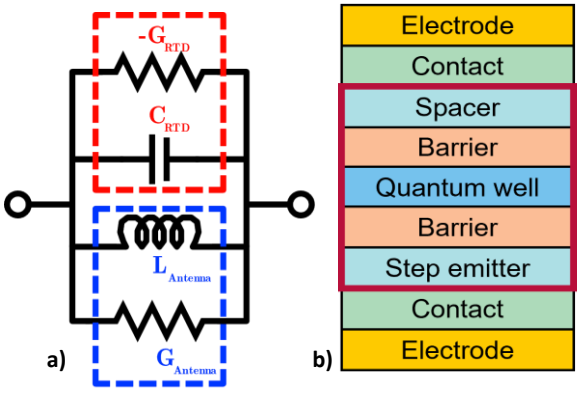

Fig. 3: *a) Small signal equivalent circuit of RTD oscillator and b) basic RTD layer structure*

higher energy levels of the quantum well enabling resonant tunneling or by thermionic emission current.

Fig. 3a shows a simplified small signal equivalent circuit of an RTD oscillator. The RTD is modeled as a capacitive device and in conjunction with an inductive antenna creates an LC circuit where the negative resistance compensates losses to enable gain and generate THz radiation. The resonant frequency of an LC circuit in its simplest form is described as $f_0 = \left[2\pi\sqrt{LC}\right]^{-1}$ so reducing the capacitance of the RTD would increase the oscillation frequency.

Fig. 3b shows the basic layer stack where the active region is highlighted in red. The capacitance is described by: $C_{RTD} = C_{geo} + C_q$ where $C_{geo} = \frac{A}{\frac{d_{QW}}{\epsilon_{QW}} + \frac{d_B}{d_B} + \frac{d_{dep}}{d_{dep}}}$ is the geometric and $C_q = -\tau_C G_{RTD}$ the quantum capacitance. A is the Area of the RTD, d and ϵ are the thickness and permittivity of the quantum well (QW), barriers (B) and depletion region (dep) which is formed by the undoped spacer layers [3,4].

Therefore, the capacitance can be reduced by increasing the spacer thickness but doing so increases the necessary bias voltage as the resistivity increases. There is also a tradeoff between lowering the geometric capacitance while increasing transit times in the depletion region so there is an optimal value depending on the target frequency. For lower frequencies the spacer should be thicker while for very high frequencies it should be thinner [5,6].

In order to better understand and predict the experimental results, a simulation with the TCAD software Sentaurus by Synopsys has been carried out. **Fig. 4** shows the band structure of the two used quantum wells. The left one consists of 4.5 nm $In_{0.8}Ga_{0.2}As$ as used in [2] while the right one uses $In_{0.53}Ga_{0.47}As$ with an InAs subwell reaching a total width of 3.76 nm. While comparable in total width, the first energy level of the quantum wells is very close which should allow a good comparison of the different material systems regarding the s-parameter measurements.

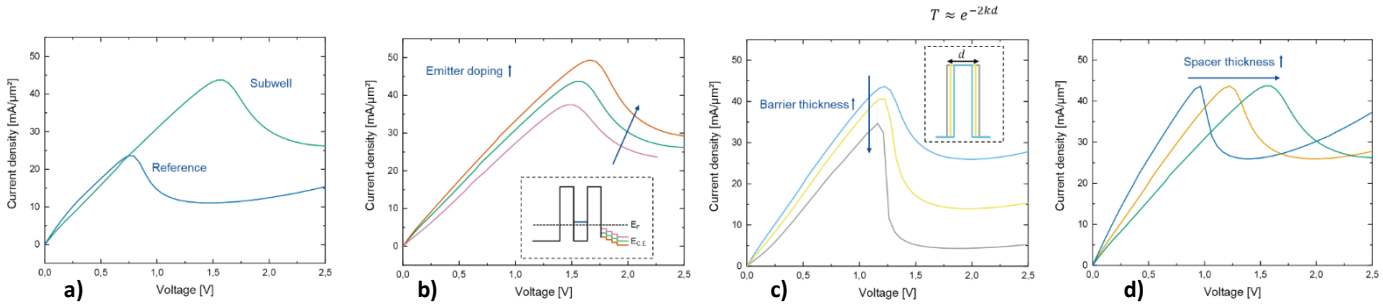

Fig. 5: *IV Simulations of* **a)** *different quantum wells,* **b)** *emitter doping,* **c)** *barrier thickness and* **d)** *spacer thickness variation*

Fig. 5 shows the effects of different layer thicknesses layers on the IV curve obtained by the simulation. The small differences between the quantum well systems still have a relatively big impact on the peak voltage as seen in **Fig. 5a**, but the higher peak current density should result in a higher power output.

As the goal is to increase current density in order to achieve higher output the emitter doping is one of the most important parameters as a higher doping increases the number of available electrons. But due to the lower conduction band edge of the emitter, the necessary bias voltage increases as well, which is shown in **Fig. 5b**. Another risk of high emitter doping is diffusion of the dopant into the quantum well structure resulting in a shorted diode. An optimal value must be evaluated [7].

Fig. 5c shows the effect of barrier thickness variation, which is another important parameter as it highly affects the transmission probability. But as thinner barriers mainly increase other transport mechanisms aside the resonant tunneling the resulting increase in valley current decreases the peak to valley current ratio (PVCR) [8] and therefore power output. But as mentioned before, a thick collector barrier increases the quantum capacitance of the RTD so for high frequencies thin barriers may be necessary.

As previously mentioned, the collector spacer thickness mainly affects the geometric capacitance of the RTD but increasing its thickness also introduces a higher resistivity which requires a higher peak voltage, which can be seen in **Fig. 5d**. It is also worth noting that a higher thickness results in an increased peak to valley voltage ratio (PVVR) which can slightly increase power output at the cost of efficiency.

Tab. 1a shows the detailed layer stack including the used electrode materials. The Ref design is based on [Ref] but the subwell quantum well is used for the parameter sweeps shown in **Tab. 1b** with reference parameters highlighted in red.

The technological concept to realize and measure the RTD is shown in **Fig. 6**. Photolithography is used to evaporate the collector metallization on the wafer which acts as the etching mask for the wet chemical etching of the RTD mesa with $H_3PO_4 : H_2O_2 : H_2O$ (1 : 1 : 25). Afterwards the emitter electrode is evaporated, and a structured resist is used to etch into the semi insulating substrate. The sideview of the resulting structure is shown in **Fig. 6a**.

To prevent a short circuit and improve mechanical stability a passivation layer shown in pink from the top view in **Fig. 6b** is structured via photolithography and etched with an O_2-plasma to reveal the collector contact.

In a last step the contact pads and feed lines shown in **Fig. 6c** are evaporated on the substrate which serve as a waveguide to perform the s-parameter measurements necessary to determine the capacitance and cutoff frequency of the RTD.

a)

	Thickness [nm]	Ref	Subwell	Doping [cm^{-3}]
	400	Au		
Electrode	10	Pt		
	10	Ti		
Contact	15	$In_{0.53}Ga_{0.47}As$		3.74E19
Spacer	25	$In_{0.53}Ga_{0.47}As$		nid
Barrier	1.2	AlAs		nid
Quantum well	1.17		$In_{0.53}Ga_{0.47}As$	
	4.5 1.42	$In_{0.8}Ga_{0.2}As$	InAs	nid
	1.17		$In_{0.53}Ga_{0.47}As$	
Barrier	1.2	AlAs		nid
	2	$In_{0.47}Ga_{0.53}As$		nid
Step Emitter	2.5	$In_{0.49}Ga_{0.51}As$		3E18
	2.5	$In_{0.51}Ga_{0.49}As$		3E18
Contact	400	$In_{0.53}Ga_{0.47}As$		2E19
	110	Au		
Electrode	10	Pt		
	10	Ti		

b)

Emitter doping	2E18 cm^{-3}	3E18 cm^{-3}	4E18 cm^{-3}
Barrier	1.2 nm	1.4 nm	1.7 nm
Spacer	10 nm	17 nm	25 nm

Tab. 1: *Epitaxial parameters of* **a)** *complete layer stack and* **b)** *parameter sweeps*

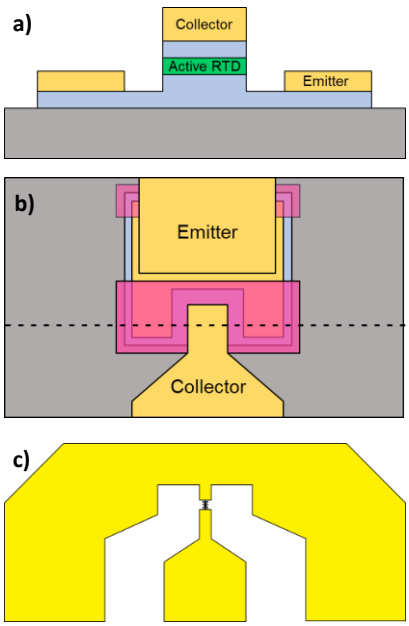

Fig. 6: *Technology concepts*

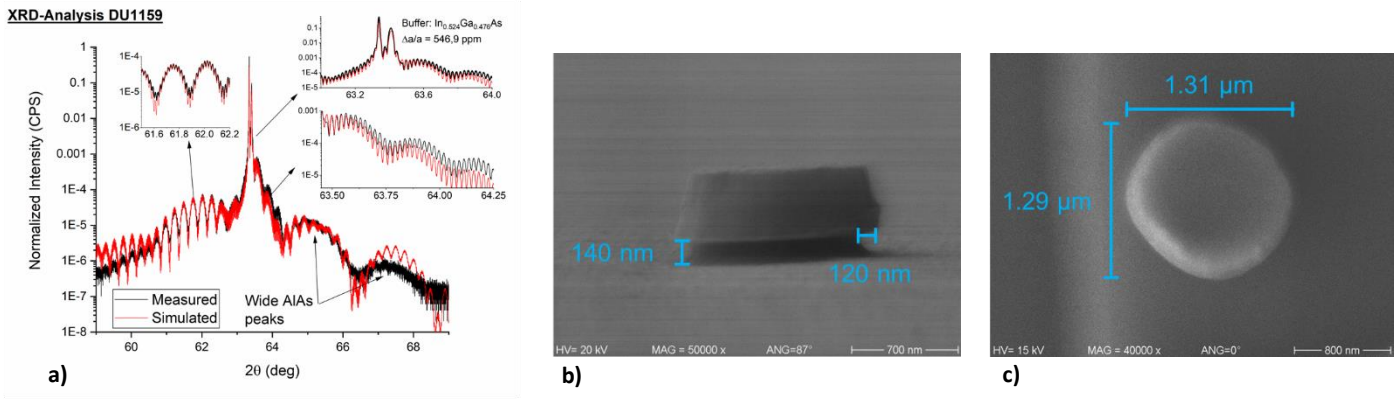

Fig. 7: a) *XRD results of MBE grown wafer and* **b)** *SEM images to determine contact area*

A single representative wafer has been analyzed by x-ray diffractometry (XRD) to evaluate the layers grown by molecular beam epitaxy (MBE). As the simulation shown in red in **Fig. 7a** shows good agreement with the black measurement curve it can be assumed that the layers are all grown as intended and the simulated IV curves should be comparable to the measurements.

The wet chemical etching process is highly isotropic, so it is necessary to determine the actual rate to be able to calculate the contact area from the electrode size.

Fig. 7b shows a sideview of the collector metal and RTD mesa which allows a generalization of the isotropy factor as its not possible to get a 90-degree view of the complete wafer. Instead, the electrode size is determined from the top view as shown in **Fig. 7c** and the contact area is obtained through the isotropy factor by measuring the vertical etch distance.

The contact area is used to calculate the current density in order to compare the measured IV curves shown in **Fig. 8a**. It is worth noting that the yield of working RTDs is very small and the measurements do not show the absolute best values possible, but it is nevertheless possible to compare them and draw conclusions for the future.

Even though the current density is not as high as expected based on the reference, values between 5-15 mA/µm² with a PVCR of around 1.5 are already a good achievement considering that thermal breakdown becomes an important issue.

The blue line represents the RTD based on the reference while the other ones use the subwell QW structure. A direct comparison can be drawn between the blue and green curve as only the QW is different.

Fig. 8b shows the simulated IV curves where the blue reference curve has been adjusted to fit the measured current density and the same parameters have been used for the other ones. It becomes clear that the RTDs with the subwell QW exhibit a way lower current density than expected, but their peak bias voltage seems to be very accurate. A possible reason for the blue curve not agreeing with the simulation could be that the indium content of the well is not as high as intended as it has not been confirmed by the XRD analysis. The simulation could also simply be wrong, but the actual reference agrees with it.

The pink curve indicates that the layer stacks can possibly reach higher current densities as the only difference between it and the green one is the emitter doping concentration, which is 2 and 3E18 cm^{-3} for the pink and green samples respectively suggesting that the green IV curve should exhibit a higher current density than the pink one.

The grey curve is the only one with 1.7 nm thick barriers instead of 1.2 nm which should result in a sharper NDR and higher PVCR like the simulation predicts, but the DC measurement shows a similar looking curve with only a slight PVCR increase compared to the green curve. The reduced peak bias voltage due to the 17 nm instead of 25 nm spacer thickness can be observed.

The blue and grey curve have very similar peak and valley bias voltages and are the only RTDs where s-parameter measurements have been successful.

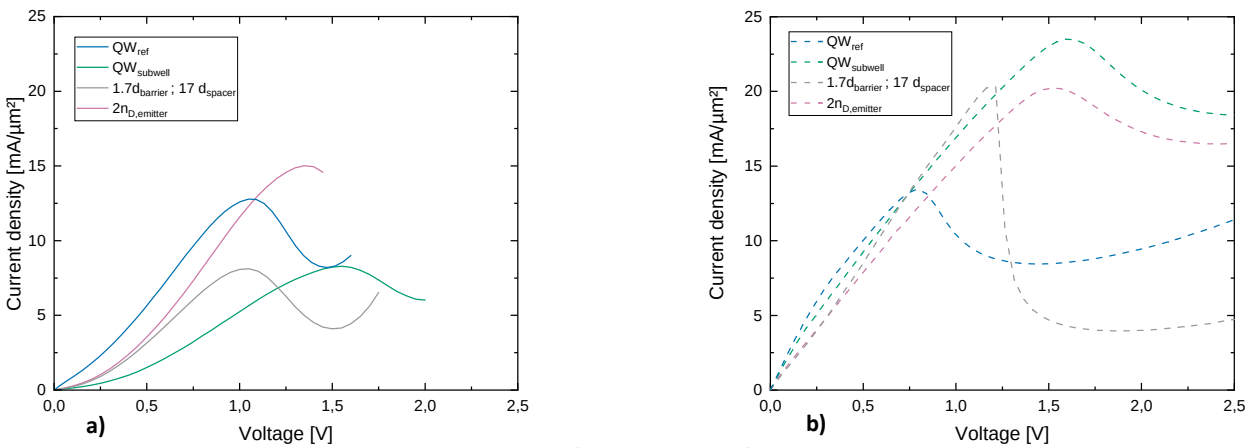

Fig. 8: *Comparison of* **a)** *measured and* **b)** *simulated IV curves*

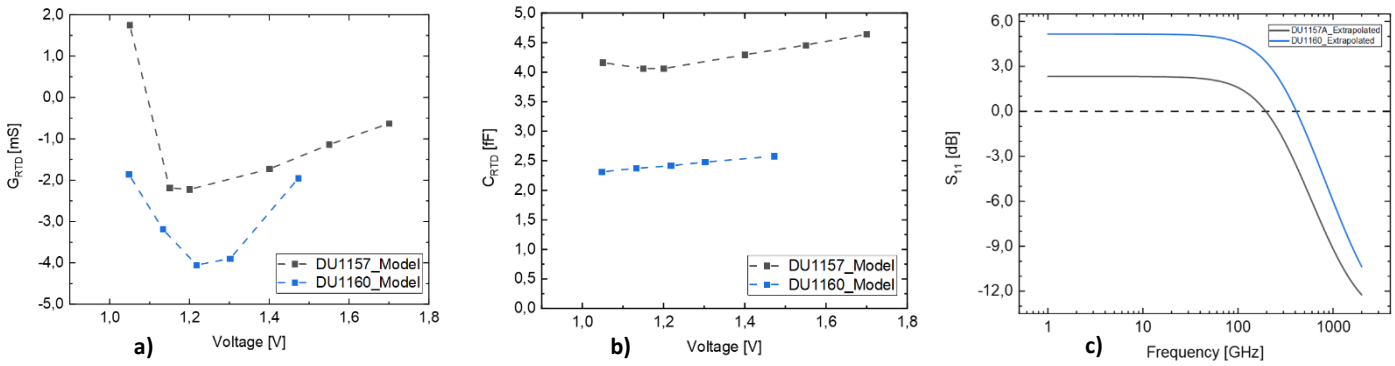

Fig. 9: a) *extracted conductance from IV-curve and* **b)** *extracted capacitance from s-parameter small signal analysis and* **c)** *extrapolated s-parameters over frequency*

Fig. 9 shows the results obtained by HF measurements. The necessary conductance to model the RTD equivalent circuit can be obtained by the derivative of the DC IV curve and is plotted in **Fig. 9a.** The minima show the turning point in the IV curve where the negative conductance is at its highest value. Most of the time this corresponds to the operational bias voltage of the oscillator. The blue reference-based sample exhibits a twice as high negative conductance as the grey sample with the subwell QW, thicker barriers and thinner collector spacer. Generally, a high negative value is desirable, but it is important to keep in mind, that a narrow NDR also reduces the possible output power of the oscillator.

The values are then used to extract the corresponding capacitance from the small signal model in **Fig. 3** by only looking at the RTD and adding the series resistance which mainly consist of the contact resistance at the collector electrode and is estimated at 75 ± 10 Ω based on previous measurements [8]. The high contact resistance is caused by the small area of around 0.2 µm² for the working devices. The results are visualized in **Fig. 9b**. Again, the blue reference-design is outperforming the subwell based RTD with its capacitance around 2 fF being half of the grey values. But this is to be expected as the grey sample has a thinner collector spacer and thicker barrier which both increases the capacitance of the RTD as mentioned before.

Extrapolating the s-parameters measured until 50 GHz allows an estimate of the possible oscillation frequency drawn by the dotted line in **Fig. 9c**. As the previous results already suggest, the blue reference designs cutoff frequency is about double that of the grey sample RTD with values of around 400 and 200 GHz respectively.

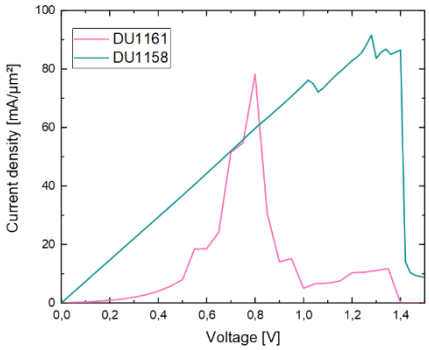

Fig. 10: *DC measurements of not working as intended RTDs*

A selection of DC measurements of not working RTD devices is plotted in **Fig. 10**. Most of the time these devices exhibit a simple resistor characteristic shown by the green curve, which corresponds to the series resistance of the used material and contact resistance of about 10-20 Ω, meaning that most likely either gold atoms or dopant diffused into the active layers therefore preventing the RTD from working properly.

Other measurements may at first seem promising but start to show undefinable characteristics and eventually break down completely. An example is given by the pink curve.

The reason for the RTDs breaking down during operation is mainly thermal degradation or possibly electromigration both caused by the relatively high current densities. The low yield can also stem from technological issues, like the before mentioned diffusion which could be caused by high temperatures of 300 °C during rapid-thermal-annealing (RTA) of the passivation structure [9].

Possible solutions are the use of a thicker platinum layer to further prevent interdiffusion of gold and indium atoms [11], a thicker collector contact layer to better protect the active layers, a lower RTA temperature to further reduce interdiffusion and buildup of indium at the contact interface.

Geometry optimizations of the RTD mesa and contacts to reduce heating of the devices may be necessary in the future to allow for bigger area sizes. Even though the capacitance is lowered by reducing the RTD area, the increasing contact resistance is a limiting factor for the high frequency operation and must be considered or further optimized as well.

Implementing an increased platinum layer significantly increased the yield of working RTD devices and extended on-wafer s-parameter measurements up to 500 GHz with the current model show a more promising f_{max} of 1.5 THz for the same layer stack previously shown in grey (DU1157). The results will be published in another work and further prove that the lower than expected performance can be improved by overcoming and optimizing the technological process difficulties.

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