Bachelor ´s Thesis in the NanoEngineering Program

Topic: Contact and Process Development for Antimony-Based Layers

Summary:

In the course of this work, antimony-based base layers for DHBT (Double Heterojunction Bipolar Transistor) applications were successfully contacted and characterized, with a particular focus on identifying the optimal surface pretreatment and metallization process. Various durations and concentrations of wet-chemical HCl pretreatments were investigated to effectively clean the semiconductor surface from native oxides. Additionally, the influence of in-situ Ar-plasma pretreatments—varying in duration and intensity—on contact quality was systematically evaluated.

A carrier concentration of 7.2×10^{19} cm^{-3} and a sheet resistance of $400\Omega/sq$ were measured. A specific contact resistance of $1.8 \pm 0.3 \times 10^{-8}\Omega cm^2$ was achieved using the Pt/Ti/Pt/Au metallization scheme, demonstrating suitability for high-frequency applications.

Furthermore, the implementation of novel TLM (Transfer Length Method) structures was pursued to enable more realistic contact characterization. The design of wire-TLM structures was established and successfully fabricated using lithographic techniques.

A PMMA bilayer resist process was developed, enabling precise control over the undercut profile and showing particular promise for low-density patterning applications. However, further optimization is required to improve its performance for high-density patterns and TLM structures. A promising approach involves reducing the difference in clearing doses between the two resist layers—achievable either by lowering the clearing dose of the top layer or increasing that of the bottom layer.

Future work will include the implementation of new test series for Ar-plasma pretreatment and the evaluation of alternative metallization schemes, particularly those based on palladium. Additionally, a slow wet-etch step—e.g., using a mixture of $H_3PO_4 : H_2O_2 : H_2O$ - may be employed to remove GaAs carry-overs and the topmost layers of the GaAsSb structure, thereby improving interface quality.