Bachelor ´s Thesis Project in the NanoEngineering Program

Topic: Optimization of Contacts on Graded Epitaxial Layers

Task:

Within the research group BHE, InP-based electronic semiconductor devices are being developed for the sub-THz and THz frequency range (0.1 – 1 THz). As device geometries continue to scale down to cross-sectional areas below 1 μm^2—particularly for Terahertz diodes and transistors—the reduction of specific contact resistance becomes crucial. While the ideal case assumes a constant RC product with scaling, practical limitations arise due to parasitic capacitances and interface inhomogeneities at the metal–semiconductor junction. Achieving successful scaling requires further reduction of the specific contact resistance through optimization of the metallization process and/or engineering of the bandgap grading in the semiconductor layer structure.

This thesis focuses on the optimization of ohmic contacts to highly n-doped InGaAs layers with a high indium content. The project involves:

1. Conceptual design of the In(Ga)As–metal interface to minimize contact resistance.

2. Optimization of the metallization process, including chemical or plasma-based surface pretreatment of the semiconductor.

3. Design and validation of low-resistance measurement techniques, including verification of test structure dimensions in the TLM (Transfer Length Method) layout.

4. Fabrication of TLM test structures using optical or electron-beam lithography.

5. On-wafer 4-probe TLM measurements using a dedicated measurement setup.

6. Data analysis of contact and sheet resistance values, with validation of the concepts developed in steps (1) and (3).