

Master's Thesis Task in the NanoEngineering Program

Topic: Development of Epitaxy of 3D GaN Nano-/Micro-Structures on Sapphire

Task:

Group III-Nitride (III/N) compound semiconductors find applications in various (opto-)electronic devices, such as light-emitting diodes, power field-effect transistors, water-splitting cells, and single-photon emitters. A particular feature of III/N semiconductors is that a spontaneous dipole moment forms along the so-called c-direction of the crystal. Depending on the crystal facet being considered, it can be polar, semi-polar, or non-polar, which in turn can affect the performance characteristics of the entire device.

The layer growth of III/N semiconductors using metal-organic vapor phase epitaxy generally occurs on sapphire in the c-direction. Thus, layer devices are exposed to the polarization field. Other facets of the crystal become accessible through the fabrication of 3D structures, rather than just layers. These 3D structures can be created directly using a bottom-up approach in the epitaxy. This involves growth through openings in a dielectric mask of a previously grown GaN layer. The highly localized growth of GaN and the choice of suitable growth parameters enable 3D-controlled growth of GaN structures in the nano- and micrometer range, which can serve as a foundation for further devices.

The goal of this master's thesis is to develop the epitaxy and technology to achieve the 3D growth of n-doped GaN structures. In the area of technology, the focus is on developing parameters for electron beam lithography to etch openings into the dielectric silicon nitride mask. The influence of the diameter and spacing of the openings on the growth will be investigated.

In the area of epitaxy, the influence of growth parameters on the 3D growth will be studied. Initially, the undoped and n-doped GaN layers must be created and characterized using suitable methods. Based on these layers, the development of growth parameters will take place, allowing for the controllable shape and size of the nano/microstructures, thus providing a suitable foundation for various devices.