

QRP PA in Switching Mode – An Exploration

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Successful projects for digital modes and CW in the HF band use final amplifiers in switching mode with digital drive, e.g. the QCX, QMX and QDX transceivers from QRP Labs or, more recently, the CW transceiver by DL1JFF. The advantages cited are simple drive using logic devices and a higher efficiency than can be achieved with linear amplifiers of the same output power. This is particularly interesting for QRP transceivers, but what is behind this, how do such amplifiers work, and what matters in their implementation?

The key to understanding is to look at the “active” element of the circuit, the transistor: In switching-mode amplifiers the transistor is driven at the gate (or base) with a rectangular pulse voltage so strongly that the drain–source (or collector–emitter) path is opened and closed like a switch. “Open” means open-circuit, while “closed” means that the transistor behaves like a short circuit. But how does amplification of the input signal arise from a mere “switch”?

What Exactly Happens in the Circuit?

To answer this question, simulating the circuit helps. Figure 1 shows the basic circuit of a switching-mode amplifier, with a transistor supplied via a choke from a battery and driven at the gate with a TTL-level pulse signal. At the drain, the output signal is coupled via a capacitor to the load resistor. As the switching transistor, an RF power MOSFET RD15HVF1 is assumed, for which the manufacturer unfortunately does not provide a SPICE model. Instead, an approximately matching, modified MOSFET model is used.

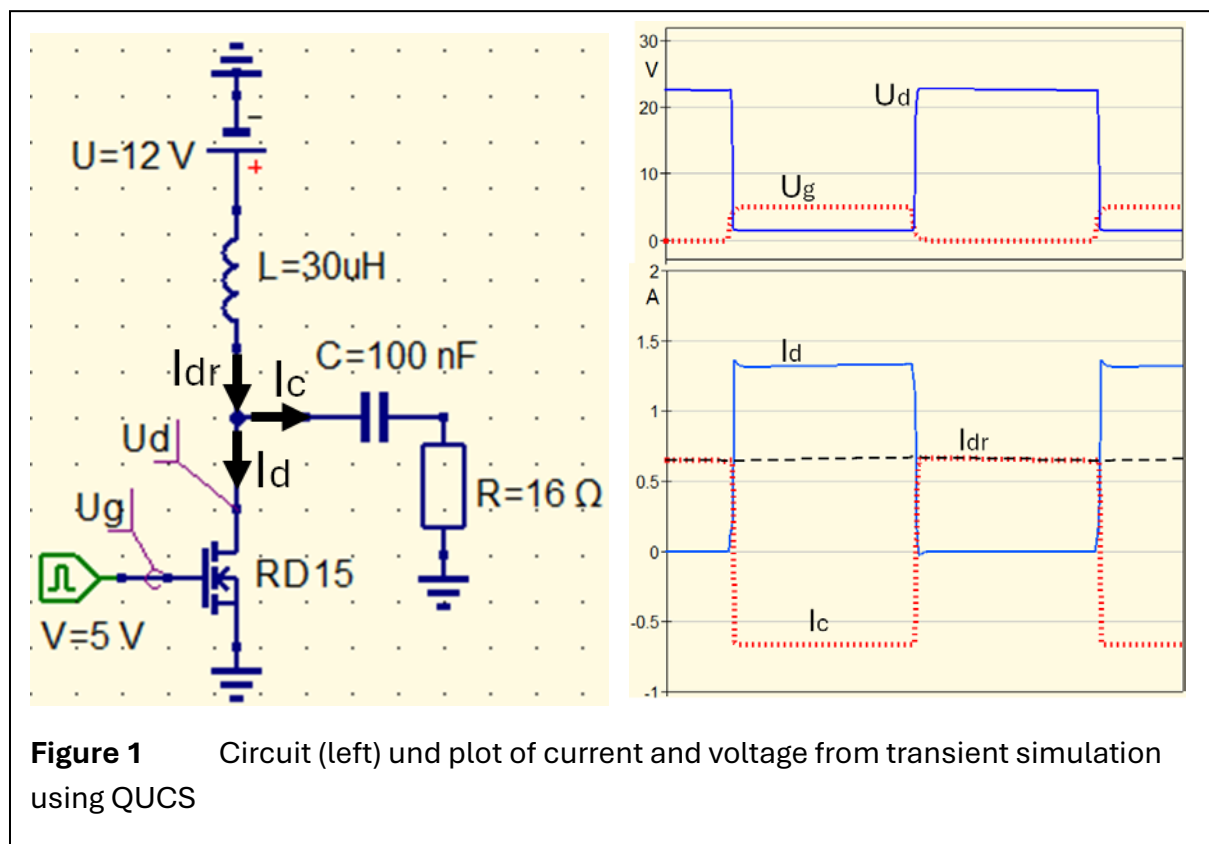
The simulation primarily reveals the relationship between the voltages and currents at the common node of choke, capacitor and transistor (the drain connection). The upper part shows the waveforms of the gate voltage U_g and the drain voltage U_d of the transistor. The lower part shows the current I_{dr} through the choke, the current I_d from the drain through the transistor to ground, and the current I_c through the capacitor to the load resistor: While the current I_{dr} through the choke is almost constant at about 0.66 A due to its high inductance, the current I_d rises to twice this value while the gate is “high”. The other half of this current comes from the capacitor – in the diagram I_c is negative, i.e. current flows from the capacitor back into the transistor during this time. As soon as the gate goes “low”, the transistor can no longer accept current, so the current from the choke must flow entirely into the capacitor – in the diagram I_c accordingly becomes positive with an amplitude equal to that of I_{dr} .

What is interesting now is $I_d = 2 \times 0.66 \text{ A}$, the current flowing through the transistor to ground. Unlike an ideal switch, the transistor exhibits a considerable “residual resistance” in the on-state – on datasheets of real switching transistors this is given as

$R_{DS(on)}$, often with values of $0.1\ \Omega$ or less. The RD15HVF1, as an RF MOSFET, is by design about an order of magnitude worse here and shows a residual resistance of approximately $R_{DS(on)} = 1\ \Omega$ in the simulation model. This produces a residual voltage of $I_d \times R_{DS(on)} \approx 1.4\ \text{V}$.

Because of this voltage, the choke causes the drain voltage U_d to rise only to $22.6\ \text{V}$. This is solely due to the “inertia” of the current flow I_{dr} through the choke, because in steady state the voltage across the choke **must average to zero (0 V) over time**; otherwise Faraday’s law would demand an increase or decrease in current. Thus, with a voltage of $1.4\ \text{V}$ in the “high” state of the drive, the voltage in the “low” state must be $U_d = 22.6\ \text{V}$ so that the average across both ends of the choke is $12\ \text{V}$. With an ideal switching transistor, which represents a short circuit in the on-state, the drain voltage would accordingly go to exactly $2 \times 12\ \text{V}$. The voltage swing at the drain is therefore only $21.2\ \text{V}$ instead of $24\ \text{V}$ in the ideal case. Because of the coupling capacitor, only $\pm 10.6\ \text{V}$ appear across the load resistor, resulting in lower output power than in the ideal case.

The problem is the voltage across the residual resistance: Here, loss power is generated in the transistor with $P_V = I_d^2 \times R_{DS(on)} \approx 1.3\ \text{W}$, however only over half a period, so that on a time average only $0.65\ \text{W}$ counts as loss power. The power balance then shows an input power (from the $12\ \text{V}$ battery) of $P_{dc} = 12\ \text{V} \times 0.66\ \text{A} = 7.9\ \text{W}$, while the output power is $P_{out} = (10.6\ \text{V})^2 / 16\ \Omega = 7\ \text{W}$, yielding an efficiency of only 88% compared to 100% with an



ideal switching transistor. The circuit could achieve higher efficiency only with a lower residual resistance of the transistor.

Why Not Use Real Switching Transistors?

This is also possible, as in the QDX final stage with four BS170 “small-signal” transistors connected in parallel. The main disadvantage of switching transistors for use in the HF band is their high gate capacitance, often hundreds of pF for power MOSFETs, which can no longer be driven by logic ICs. In contrast, the RD15HVF1 with 54 pF can easily be driven at the gate by two TTL gates connected in parallel (e.g. inverters or AND gates).

Experimental Investigation

To see the behavior of the circuit “live”, I built the amplifier, Figure 2: The RD15HVF1 is supplied with DC from 12 V via an RF choke. A logic circuit with TTL levels between 0 and 5 V generates the gate voltage U_g and switches the transistor at 3.6 MHz. The AC component of the drain voltage U_d is coupled via a capacitor to the load resistor $R = 16\ \Omega$, formed from three power resistors in parallel. In operation, the circuit draws a current of 0.61 A from the 12 V supply. Using probes, the gate voltage U_g and the drain voltage U_d are measured – the oscilloscope in Figure 3 shows the voltage waveforms.

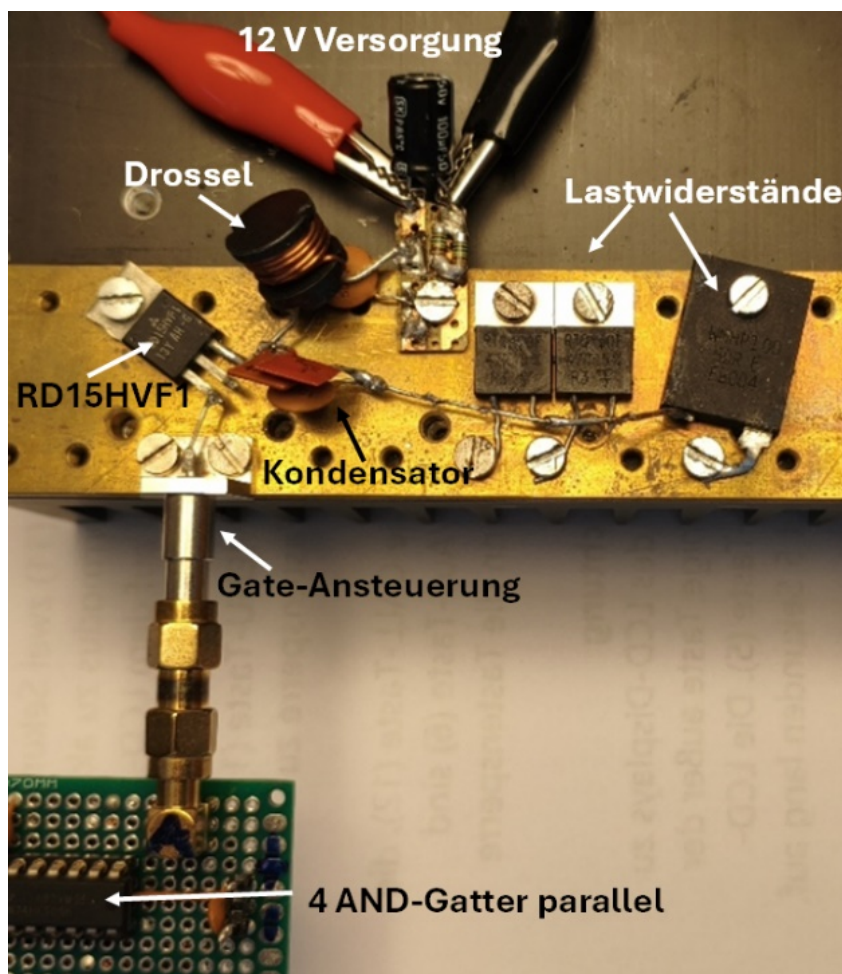


Figure 2 Test circuit with RD15HVF1 and TTL-level drive.

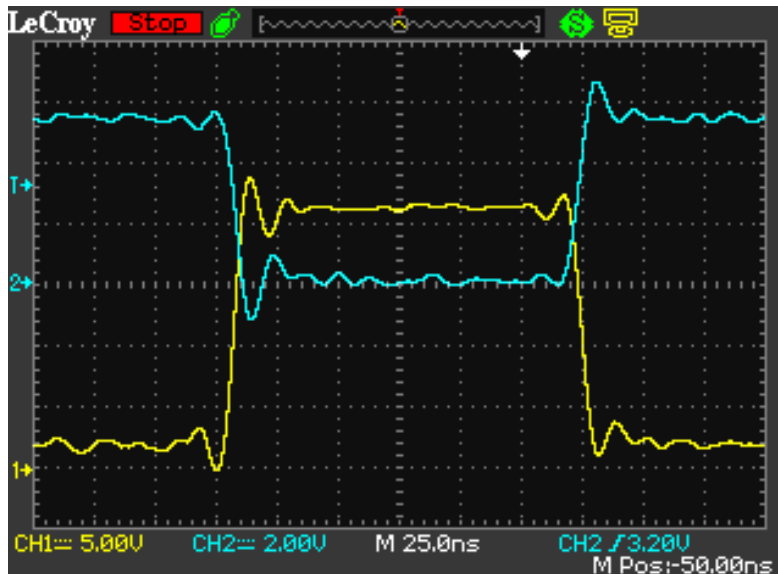


Figure 3 Waveforms of the voltages at the gate (U_g in blue) and at the drain (U_d in yellow).

One can see for both voltages a pulse shape with steep edges but in opposite phase: When U_g goes to 5 V (“high”), U_d goes down, and when U_g goes “low”, U_d rises to a high voltage. At the drain voltage, the voltage swing is of interest: While the gate is “low”, the drain voltage shows about 22 V, and while the gate is switched “high”, a residual voltage of about 2 V remains. Compared to the simulation model, the residual resistance is apparently significantly higher, at about 1.6 Ω . The voltage swing at the drain reaches 19 V, so that at the load resistor with ± 9.5 V across 16 Ω an output power of 5.6 W is obtained. Compared to the input power of 12 V $\times$ 0.61 A = 7.3 W, about 1.8 W are lost, of which 1.2 W are due to the residual resistance of the transistor.

Switching-Mode Amplifier with Filtering

The spectrum of a pulse signal with symmetrical rectangular pulses theoretically shows an infinitely extended spectrum with a spectral line at the fundamental frequency and further lines at odd-order harmonics, whose amplitudes decrease with the inverse of their order. The fundamental contains about 81% of the total signal power, corresponding to approximately -1 dB, and all harmonics together the remaining 19%.

The experimental signal in Figure 3, unlike an ideal rectangular pulse, shows overshoot at the transitions, caused by a series inductance of about 20 nH from the assembly of the load resistors. The steep edges of the drive excite, at each transition from the blocked to the conducting state of the transistor, additional high-frequency oscillations in the circuit that are not visible in the oscillogram due to bandwidth limitation; although they decay again after each transition, they significantly fill up the output spectrum, Figure 4, compared to that of a symmetrical rectangular pulse.

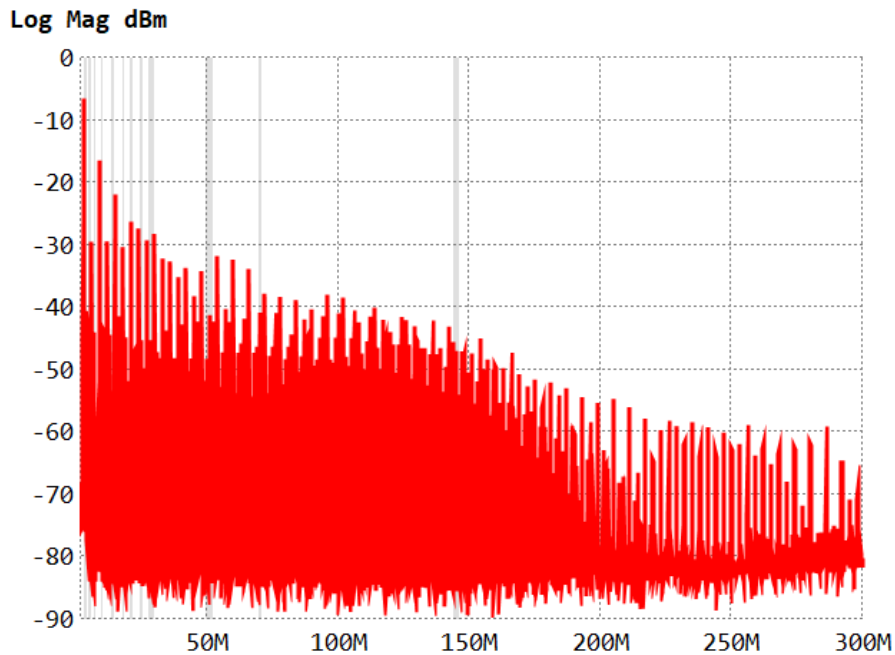


Figure 4 Spectrum of the signal in Figure 3.

It is clear that this output signal must not reach the antenna – the spectral components above the fundamental frequency must be attenuated. This could be done with a diplexer filter that routes the fundamental to a matched antenna and all harmonics to a matched termination resistor. The input impedance of the filter would then be the same for all frequencies and equal to that of the load resistor in the circuit. The circuit would therefore work exactly as with the load resistor alone, except that 19% of the output power would be uselessly lost.

If one wants to avoid this loss, an LC bandpass or low-pass filter is used to suppress the harmonics. However, the input impedance of the filter is equal to that of the original load resistor only for the fundamental; for frequencies above it, it is almost purely reactive and cannot absorb power. This leads to different behavior of the circuit, as can be seen in Figure 5. Here, a resonant circuit for 3.6 MHz consisting of $L = 0.4 \mu\text{H}$ and $C = 4.7 \text{nF}$ was connected in parallel to the load resistor. The residual voltage when the transistor is conducting (gate is “high”) is significantly higher than in the original circuit and its waveform is distorted. At the same time, the drain voltage is sinusoidally shaped by the resonant circuit, and also somewhat increased. The originally rectangular pulse has become almost a half-sine wave, albeit slightly widened. In particular, at the transition from the blocked to conducting transistor (gate voltage jumps from zero to 5 V), the drain voltage has not yet fallen completely to zero while the transistor already conducts current due to the high gate voltage. This is the cause of additional power losses (heat) in the transistor. To analyze this situation, after measuring the spectrum of the bandpass-filtered signal in Figure 6, a transient simulation is shown again.

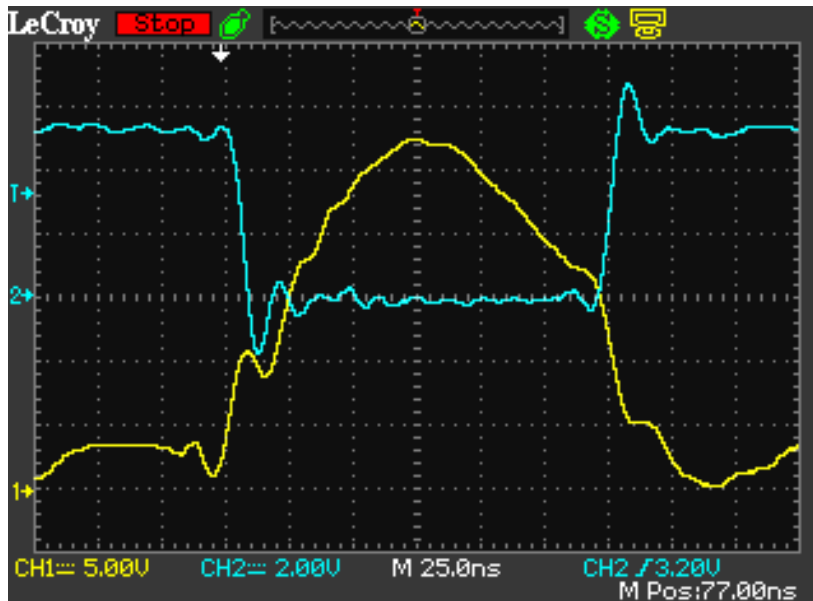


Figure 5 Voltages at the gate (in blue) and at the drain (in yellow) with the load resistor loaded by a parallel resonant circuit.

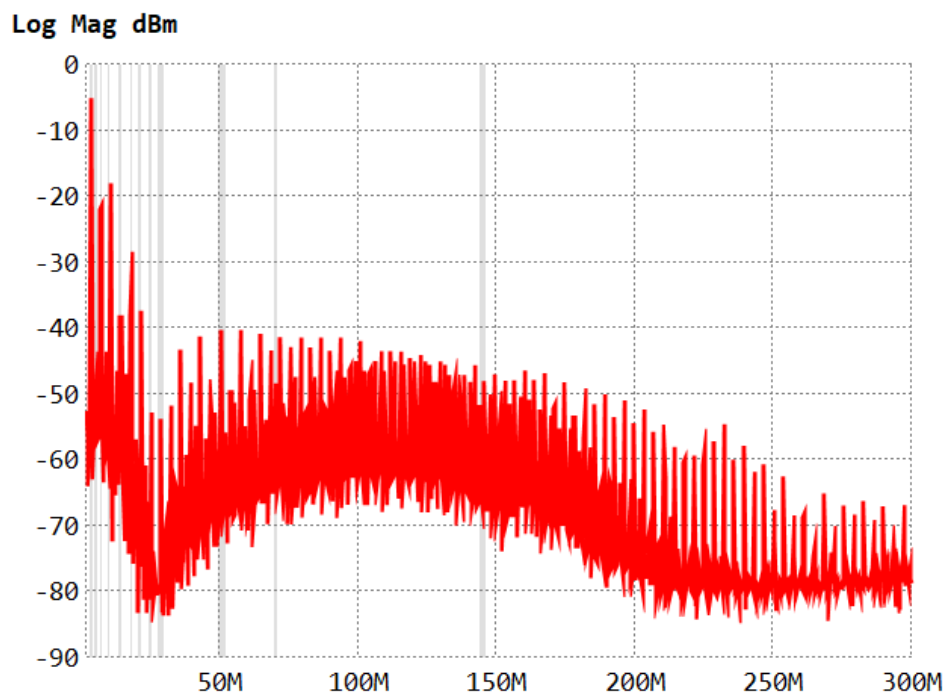


Figure 6 Strongly reduced harmonics in the spectrum of the amplifier output signal with a parallel resonant circuit.

The circuit of the amplifier with an LC resonant circuit for filtering is shown in Figure 7. The results of the transient simulation next to it primarily reveal the relationship between the voltages and currents in the circuit.

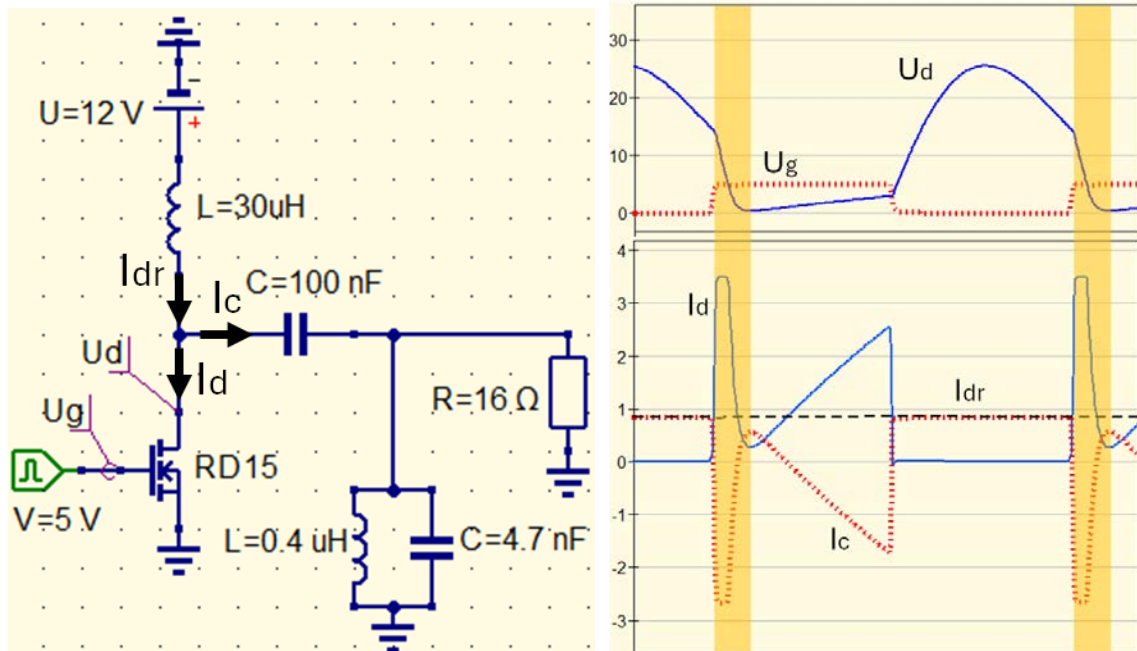


Figure 7 Switching-mode amplifier with LC resonant circuit.

During the half-period with $U_g = 0$, no drain current flows, and even in the simulation the drain voltage shows a half-sinusoidal waveform, whereas without the resonant circuit a rectangular waveform existed. In the other half-period, when the gate is “high”, the residual voltage first falls and then rises again to over 2.5 V, where in the case without the resonant circuit only a constant 1.4 V was seen (it should also be noted that in the simulation the amplifier now draws 0.83 A instead of 0.66 A). The waveform of the residual voltage results directly from the waveform of the drain current: As soon as the gate voltage goes “high”, the transistor conducts and, in a short pulse, carries a high current that is largely drawn from the capacitor. This region is highlighted in yellow in the diagram. Afterwards, the drain current transitions to a linear rise as when “discharging” an inductance, until the end of the half-period when the gate voltage falls to zero.

In the yellow-highlighted part of the diagram, an important process leading to power losses becomes apparent: While the drain voltage steeply falls from 15 V to zero within about 5% of the period, a high current of 3.5 A flows through the transistor. This results in high loss power (heat) in the transistor during this time; roughly estimated on average as $3.5\text{ A} \times 6\text{ V} = 21\text{ W}$. Although this loss power occurs only once per period with a duty cycle of 5%, it results in an average loss power of 1 W, which significantly degrades the amplifier’s efficiency.

From Switching-Mode Amplifier to Class E Operation

With Class E operation, an improvement in efficiency is pursued by reducing the losses in the yellow-highlighted transition. Ideally, the drain voltage has already fallen to zero when the transistor is switched on by the gate voltage. In the present circuit, L and C can be varied for optimization, i.e. the resonant frequency and (loaded) Q of the resonant circuit. The simulation finds a good halving of the loss power when increasing the Q and simultaneously increasing the resonant frequency of the resonant circuit, e.g. with $L = 0.5 \mu\text{H}$ and $C = 2 \text{ nF}$. However, it turns out that an ideal shape of the drain voltage cannot be achieved with these two variables without simultaneously increasing the losses due to the residual voltage – a further degree of freedom in the network is missing here.

This can be provided by a (low-pass) circuit of higher order (greater number of reactances):

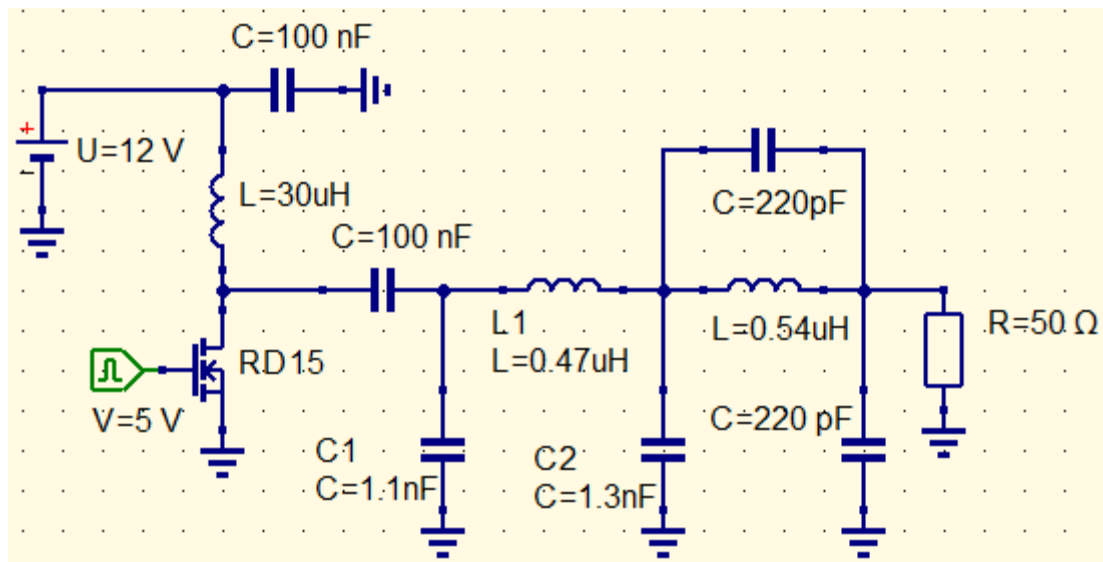


Figure 8 Circuit of a Class E amplifier with a transforming low-pass filter for 7 MHz.

Figure 8 shows the schematic of another experimental circuit, which was implemented on a PCB for the 40 m band. The low-pass filter, consisting of four capacitors and two inductors, transforms the 50Ω load resistor down to the region around 11Ω . The combination of $C1$, $C2$ and $L1$ ensures that at 7 MHz the impedance “seen” by the transistor at $C2 = 1.0 \text{ nF}$ is purely real, i.e. with approximately $Z_D \approx 10 \Omega$ has no reactive component. Increasing $C2$ to 1.66 nF adds an inductive component with $Z_D \approx (11.5 + j5.1) \Omega$, and with $C2 = 2 \text{ nF}$, $Z_D \approx (12 + j12) \Omega$. These inductive components essentially determine the shaping of the drain voltage, as the measured drain voltage waveforms of the experimental circuit in Figure 9 show. With increasing capacitance of $C2$, the pulse shape of the drain voltage becomes both more rounded and shortened and shifted.

The output power of the amplifier circuit was also clearly dependent on $C2$. Although the associated waveform of U_d does not yet appear optimal for Class E operation, $C2 = 1.66 \text{ nF}$ yielded the highest power of 5.9 W at a maximum efficiency of 59%, including the

losses in the choke and the filter. In this configuration, the amplifier can also be connected “to the antenna”, since the transforming low-pass filter also sufficiently attenuates the harmonics, as the output spectrum in Figure 10 shows.

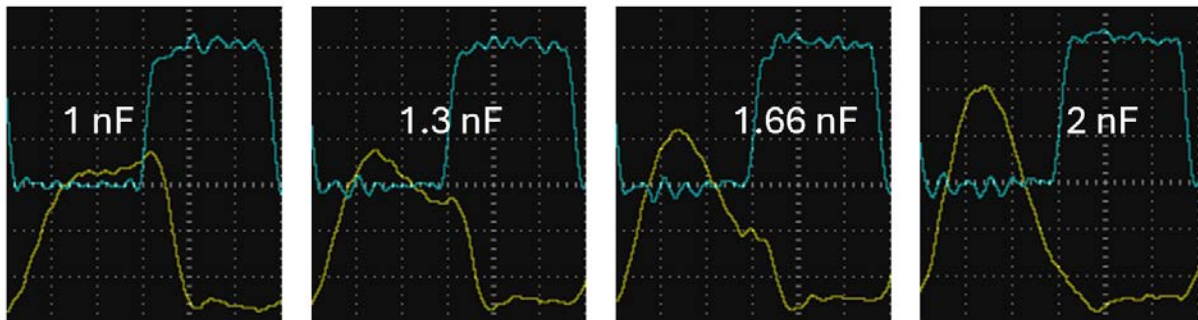


Figure 9 Measured drain voltage waveforms (in yellow) at 7 MHz for different values of C2. Gate voltage in blue.

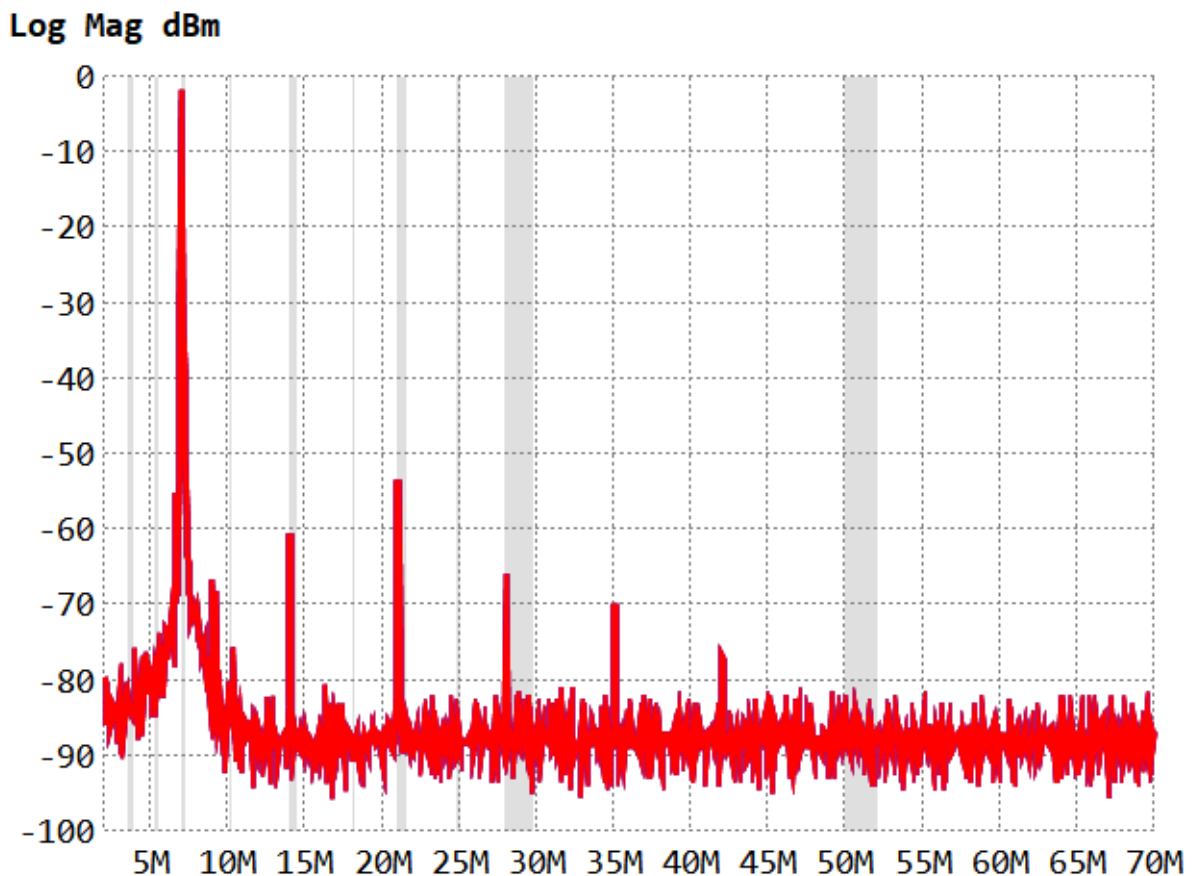


Figure 10 Spectrum at the amplifier output, measured behind a 40 dB attenuator.

References

QRP Labs: QDX Assembly Manual, <https://qrp-labs.com/qdx.html>

Hartmut Linke, “CW Transceiver with Binaural Receiver and Class E Final Stage”, *Funkamateur*, 5/2026, pp. 364–368.