

Aufgabe der Abschlussarbeit im
ISE Masterstudiengang

für: Herrn Adam Rydygier

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Thema: Design and Implementation of an Area Efficient Low-Power Multistage Decimation Filter Technique for a 2nd Order Delta-Sigma A/D Converter

Thesis Task:

During the past decades Delta-Sigma Analog-to-Digital Converters (DS ADC) have drawn great attractions due to their high linearity and high Signal-to-Noise Ratio (SNR) as well as their high resolution. Unlike traditional A/D converters, where one has to put additional design effort into their building blocks in order to obtain an overall high accuracy, oversampling and noise-shaping features employed in DS ADC's allow to swap speed for accuracy. In this way, making it insensitive to imperfections on the analog circuitry and thus allowing to relax on the circuit implementation of this part. Now, in order to cope with future CMOS technology trends it has become of huge importance to downsize the area requirement and preserve good power efficiency of such a design.

A 2nd order discrete-time single bit DS Modulator, intending to provide measurement data like e.g. power and temperature in a System-on-Chip (SoC) design, has been designed in a previous master thesis at IMST and individual analog blocks have been partially layouted using 130 nm CMOS technology. Based on this design and thus for completing the project a proper decimation filter has to be come up with as well as designed and implemented. The elaboration of the thesis should meet the following criteria:

- Research of literature regarding applicable decimation filter topologies with respect to the actual specification.
- Implementing, simulating and validating a behavioural model of an appropriate filter topology with the help of Matlab/Simulink Tool.
- Coding the RTL model of the decimation filter in VHDL and synthesizing with Cadence RTL-Compiler in an advanced CMOS technology.
- Adapting the current DS modulator to the actual specifications and porting it to an advanced CMOS technology with Cadence Virtuoso.
- Layouting the Top level of the whole DS ADC design.
- Performing mixed-signal simulation on the final design for verification.

After completion of thesis work a public presentation of results is to be given at the department.