3 ns single-shot read-out in a quantum dot-based memory structure

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Fast read-out of two to six charges per dot from the ground and first excited state in a quantum dot (QD)-based memory is demonstrated using a two-dimensional electron gas. Single-shot measurements on modulation-doped field-effect transistor structures with embedded InAs/GaAs QDs show read-out times as short as 3 ns. At low temperature ($T = 4.2$ K) this read-out time is still limited by the parasitics of the setup and the device structure. Faster read-out times and a larger read-out signal are expected for an improved setup and device structure. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4864281]

Self-organized III-V quantum dots (QDs)[1] are ideally suited for charge storage devices.[2–7] The QDs are used as storage nodes that are embedded into a modulation-doped field-effect (MODFET) structure which is used to perform the write, erase, and read operations.[6] The QDs offer large confinement potentials which could facilitate long storage times up to non-volatility (more than ten years).[8] Large localization energies up to 800 meV have already been demonstrated[8] and enable storage times up to 1.6 s at room temperature.[9] The write times in such a QD memory with InAs/GaAs and GaSb/GaAs QDs equal those of the DRAM.[10] Proof of fast read-out of the charge state of such QD-based memories is yet missing.

In this letter, we use the time-resolved transconductance spectroscopy method[11–13] to determine the s and p electron charging states of self-organized InAs/GaAs QDs embedded in a modulation-doped field-effect transistor (MODFET). The conductance change of the 2DEG for QDs filled with two or six electrons enables us to detect the charge state in a very fast single-shot experiment, with read times down to $\sim$ 3 ns for both charge states.

In a simple Drude model, the coupling between QDs and the 2DEG is determined by two factors.[14,15] First, the electrons confined in the QDs act as a scattering Coulomb potential for the electrons in the 2DEG channel and result in a decreased mobility. Second, the QDs resemble a quantum capacitance, originally introduced by Luryi for quantum wells,[16] by which the electrons in the QDs deplete the 2DEG of carriers through capacitive coupling (field effect). Both effects combined reduce the conductance of the channel, which can be measured directly via the source-drain current

$$I_D(t) = \frac{q \times w}{l} \times n_{2DEG}(t) \times \mu_{2DEG}(t) \times V_D(t), \qquad (1)$$

where q is the elementary charge, w the width, and l the length of the channel, n_{2DEG} the electron area density in the 2DEG, μ_{2DEG} the electron mobility in the 2DEG, and V_D the applied drain voltage. In the following experiments we will use the change in $I_D(t)$ of the 2DEG to distinguish between QDs charged with zero, two and six electrons in our MODFET.

The device is grown by molecular beam epitaxy (MBE). A schematic depiction is shown in Fig. 1(a). On top of an n-GaAs substrate a GaAs buffer layer of 200 nm is deposited, followed by an AlAs/GaAs superlattice with 40 pairs of 2/2 nm width. Then, $Al_{0.34}Ga_{0.66}As$ is grown, and after 300 nm an n-type Silicon δ-doping is introduced with a nominal areal density of 3×10^{12} cm^{-2}. After a 16-nm-wide $Al_{0.34}Ga_{0.66}As$ spacer layer, 15 nm of GaAs are deposited in order to form the quantum well, which contains the 2DEG. To create a tunneling barrier between the 2DEG and the QDs, 10 nm of $Al_{0.34}Ga_{0.66}As$ are grown, followed by 5 nm GaAs, after which the InAs QDs are grown in the Stranski-Krastanov growth mode with a nominal areal density of 3×10^{10} cm^{-2}. The QDs are capped by 30 nm GaAs which is then covered by a 29-pair AlAs/GaAs (3/1 nm) superlattice, and finally capped by 5 nm GaAs to prevent oxidation.

The structures are processed as 3-terminal devices by standard electron-beam lithography and standard chemical wet-etching techniques using Ni/AuGe/Ni (6/230/50 nm) and subsequent 15-min-ramped-up annealing for 1 min at 440 °C for the Ohmic source and drain contacts, and Ti/Au (12/250 nm) as gate (Schottky) contact. The gate area is $5 \times 100\ \mu m^2$. With the nominal areal density of the InAs QDs (3×10^{10} cm^{-2}), a total number of about 150 000 QDs are present under the gate. Hence, the total charge that is transferred lies between 24 fC (1 electron per dot) and 144 fC (6 electrons per dot). The source-drain resistance is about 1 kΩ. The advantage of the present device design is its down-scaling potential, such that eventually only a few or even a single QD can be used for storage.

With a confinement potential of ~200–300 meV, the storage time of electrons in InAs/GaAs QDs is not sufficient to perform measurements at room temperature,[9] hence the read time is measured at a temperature of 4.2 K. This limitation has no effect on the read-out measurement, because in the present device charge transfer takes place by tunneling. The method employed to determine the read times is schematically shown in Fig. 1(c). First, by the application of the preparation pulse, the QDs are prepared to their initial state (charged or uncharged) with a specific number of electrons. The number of electrons stored in the QDs and the corresponding gate

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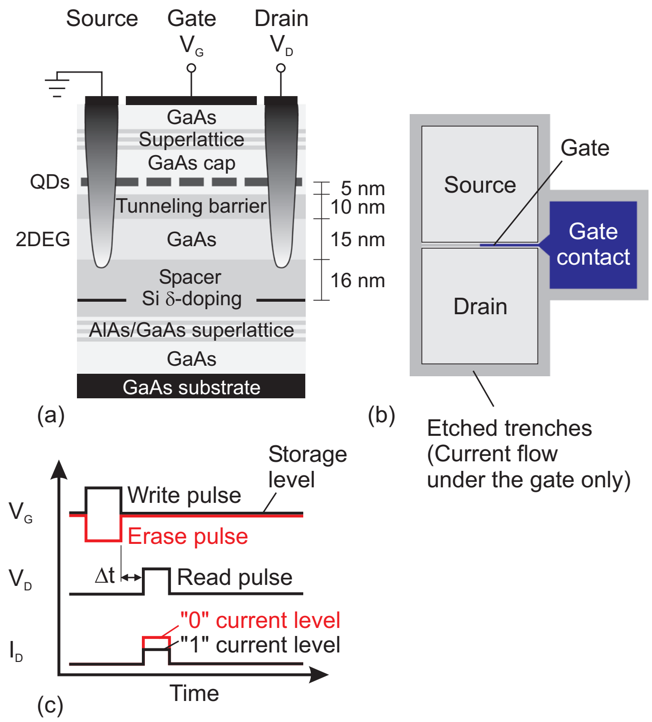

FIG. 1. (a) Schematic sample structure. (b) Gate, source, and drain contact layout. The gate has an area of $5 \times 100\,\mu m^2$. The dark shaded areas mark trenches etched below the 2DEG in order to suppress current flow other than under the gate. (c) Read time measurement method. The read pulse follows the preparation pulse after a delay time Δt.

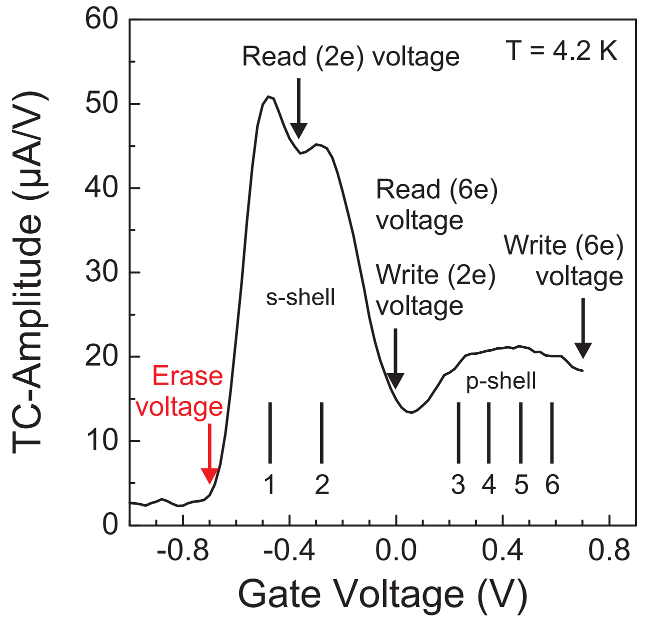

FIG. 2. Transconductance versus the gate voltage at 4.2 K. The curve resembles the charging spectrum of the QDs with one to six electrons per dot. The erase voltage, the two write voltages for two-electron and six-electron charging, and the two read voltages are indicated in the graph.

voltages were determined before by transconductance spectroscopy (for details, see Refs. 11–13). The charging spectrum for the electrons is shown in Fig. 2. When the gate voltage V_G is increased from -1 V to 0.7 V, the QDs are successively charged with one to six electrons, which can clearly be seen as two distinct peaks corresponding to the two electrons in what is sometimes called the s-shell, and a single plateau-like feature which corresponds to the four-electron charging peaks of the so-called p-shell,[17–19] where the splitting of the p-states cannot be resolved. With increasing gate voltage, the tunneling barrier between the QDs and the 2DEG is decreasing. As a consequence, the time constants of the tunneling processes decrease with increased occupation of the dots. They range from some milliseconds for the s-shell electrons to just microseconds for the p-shell electrons. Fitting a Gaussian to the first peak results in a standard deviation of 70 mV, which can be converted by using the lever arm of 6 to a standard deviation of 12 meV for the first energy level of the QD ensemble. Since the confinement potential is limited mainly by the localization in the growth direction, the latter value directly indicates the height variation of the QDs in the ensemble.

The initial voltages are chosen here to define two different charging conditions (see Fig. 2). In equilibrium the QDs are completely empty at a gate bias $V_G = -0.7$ V, which is chosen as erase voltage. Then, in a first step, the QDs are charged with only two electrons (2 e) at a gate bias $V_G = 0$ V. The read-out of the charge state of the QDs is then done at a gate voltage of -0.4 V. In a second step, the QDs are charged with six electrons (6 e). The erase voltage is the same as for the two-electron case, but the write voltage is now at $V_G = 0.7$ V and the read-out voltage at $V_G = 0$ V.

After the preparation, the gate voltage is set to the read-out voltage, and after a delay time $\Delta t = 1\,\mu s$ the conductance of the source-drain channel is measured by applying a short read pulse V_D with an HP8131A pulse generator to the drain contact while keeping the source contact grounded. During the read pulse, the current through the 2DEG is measured in a time-resolved measurement scheme by a Femto DHPCA-100 current amplifier with 200 MHz bandwidth, and the equivalent voltage is recorded by a National Instruments NI-PCI-5122 SCOPE card with 2 Gigasamples per second (in sampling mode) with 100 MHz bandwidth. Depending on the charge state of the QDs, either a larger (QDs uncharged) or a smaller (QDs charged) source-drain current is measured. By successive reduction of the read pulse width, the read time limit is determined. The read time limit is defined as the shortest time interval that still allows to distinguish between the different charging states.

Figure 3 shows the read time measurements for two different initial charge states of the QDs (the 2e- and the 6e-charge state) and different read pulse widths ranging from 10 ns down to 1 ns in single-shot measurements. After charging the QDs with two electrons each (Fig. 3(a)), the hysteresis opening between the two states is 6%–7%[20] for a read pulse width down to 3 ns at a drain voltage of $V_D = 80$ mV. When the read pulse width is decreased to 1 ns, the charge state of the QDs cannot be discriminated anymore. Hence, the estimate for the minimum read-out time in the present device is 3 ns. The signal-to-noise ratio (SNR) for the hysteresis signal (difference between the current curves for the uncharged and charged state) increases from values of 3.7 (3 ns) to 7.4 (10 ns).[21] Figure 3(b) shows the single-shot read time measurement after the QDs have been charged with an average of 6 electrons per dot for read pulses between 1 and 10 ns. Again, the charge state cannot be determined with the 1-ns pulse, but a pulse of 3 ns width can securely distinguish

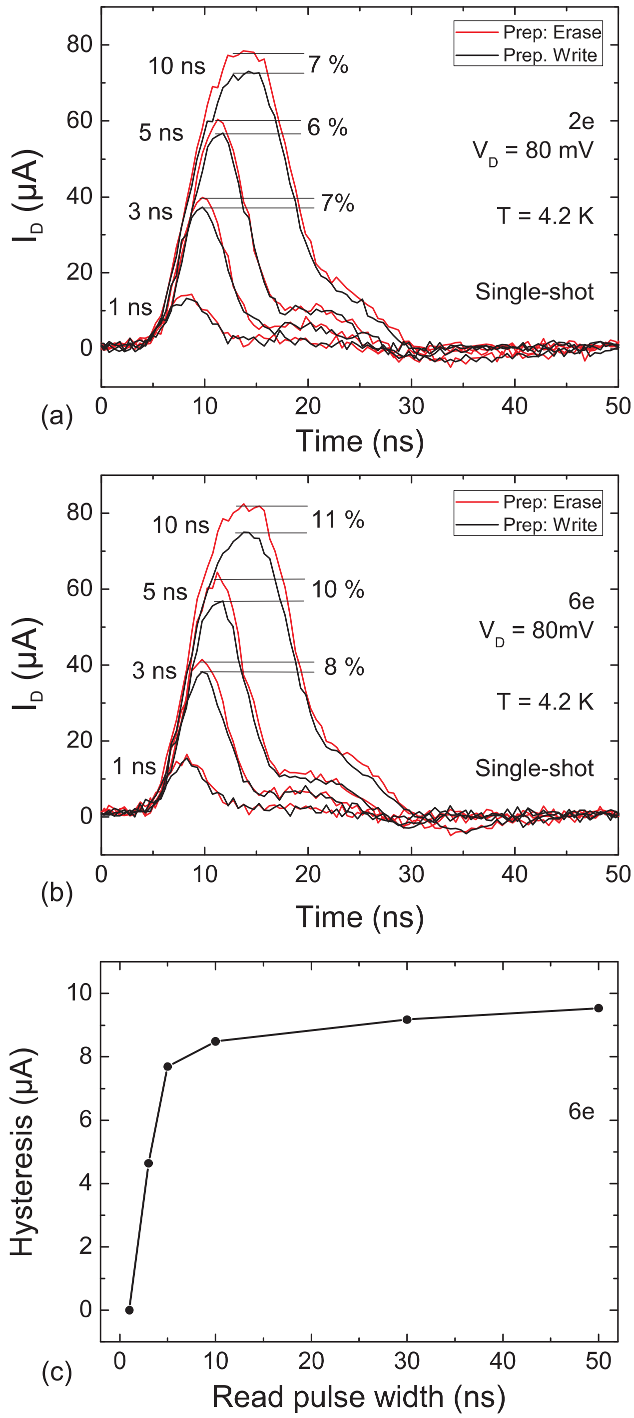

FIG. 3. Read time measurements: source-drain current I_D as a function of time for different read pulse widths. (a) QDs with an average charge of two electrons per dot in a single-shot measurement. (b) QDs with an average charge of six electrons per dot in a single-shot measurement. (c) Hysteresis opening of the six-electron measurement as a function of the read pulse width.

between charged and uncharged dots. When the pulse width is increased to 10 ns, the hysteresis opening increases to 11%. This is due to the increased number of charges in the QDs. However, the increase in hysteresis opening is less than one would expect due to the threefold increase in charge in the QDs. This sublinear behavior is due to the much smaller storage time of the p-shell electrons (the energy difference between s- and p-shell is about 50 meV) which partly have been reemitted already before starting the read time measurement. Then, as in the two-electron read time measurement, the estimate for the minimum read time required is 3 ns. The SNR for the hysteresis signal increases from values of 4.6 (3 ns) to 8.5 (10 ns).

Although the amplitudes of the read voltage pulse V_D in the measurements were all set to 80 mV, they induce a current which is increasing with increasing pulse width. This indicates that the sample and/or the setup are operated close to their cut-off frequency. This can be seen in Fig. 3(c), which shows the hysteresis opening for the six-electron measurement as a function of the read pulse width up to 50 ns. It can be seen, that the hysteresis opening saturates with a larger pulse width. Hence, the measurement is limited by the parasitics of the device and the setup. The steep increase and saturation around a pulse width of 10 ns corresponds well with the bandwidth limitations of the current amplifier and the sampling card we used. With an optimized setup, a read-out with a much smaller pulse width should be possible. To increase the signal difference between charged and uncharged QDs visualized in the source-drain current I_D, the distance between the QD layer and the 2DEG channel should be made as small as possible. However, the possible maximum increase in the capacitive coupling effect would only be about 20% (estimated for a simple equivalent circuit model[22]). Yet, this is only possible if the confinement potential is increased simultaneously, such that tunneling leakage does not prevent any charge storage in the QDs. Also, to further increase the coupling effect, the area covered by QDs with respect to the uncovered area should be made as large as possible.[23,24] Ideally, the channel width should be decreased such that only a single QD fits on top of it. A larger increase in the read-out signal can be achieved, if the carrier concentration in the 2DEG is decreased. This will, however, also affect the resistance of the channel and might result in adverse effects in the parasitics.

In summary, we have demonstrated fast electrical read-out of the charge state in an InAs/GaAs quantum dot memory structure by a single-shot read pulse down to 3 ns at a temperature of 4.2 K. Both charge states investigated (two and six electrons per dot) exhibit the same read time limit. We conclude, that this limit presents an upper bound and is still the result of the parasitics of the setup as we observe a decreasing pulse height when reducing the read pulse width. Optimization of the setup should allow a much faster read-out. A modified structure having a 2DEG with lower charge carrier density will improve the read-out signal. Our results show, that a 2DEG underneath a layer of self-organized QDs can be used as a very fast detector for the read-out in a memory structure with just a few electrons per QD.

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